Data book

MH2103Cxxxx

Enhanced, truly random number, hardware encryption algorithm unit, 32-bit Arm? Cortex-M3 core microcontroller with 128K/ 256K byte flash 10 timers, 2 ADCs, 2 Dacs, 10 communication interfaces

Features:

- Kernel: 32-bit Arm?Cortex?-M3Core
  - The maximum operating frequency is 216MHz 2.54DMips/MHz(CoreMark1.0)
  - Single cycle multiplication and hardware division
- Memorizer
  - 128K/256K bytes of flash program memory
  - 32K/64K bytes of SRAM
- Clock, reset, and power management
  - 2.0 to 3.6 volts power supply and I/O pins
  - Power-on/power-off reset (POR/PDR), Programmable Voltage Detector (PVD)
  - 4 ~ 16MHz crystal oscillator
  - Built-in factory-tuned 8MHz RC oscillator
  - Inline calibrated 40kHz RC oscillator
  - 32kHz RTC oscillator with calibration
- Low power consumption
  - Sleep, downtime, and standby modes
  - VBAT powers the RTC and the backup register
- 2 12-bit analog-to-digital converters, 1us conversion time (up to 10 input channels)
  - Conversion range: 0 to 3.6V
  - Temperature sensor
- 2 12-bit D/A converters
- DMA: 12-channel DMA controller
- Debug mode
  - Serial single-wire debugging (SWD) and JTAG interfaces
  - Embedded Tracking Module (ETM)
- I/O port
  - 37 multifunctional bidirectional I/O ports, all of which can be mapped to 16 external interrupts
  - All GPIOs can be forcibly configured with a pull -down resistor
- Enhanced CRC computing unit
- 10 timer
  - 4 16-bit timers, each with up to 4 channel and incremental encoder inputs for input capture/ output comparison /PWM or pulse counting
  - 1 16-bit PWM advanced control timer with dead zone control and emergency brake for motor control
  - 2 watchdog timers (standalone and window)
  - System time timer: 24-bit self-decrement counter
  - Two 16-bit basic timers
- 10 communication interfaces
  - Two I2C ports
  - 3 USART interfaces (support ISO7816, LIN, IrDA interfaces and modem control)
  - 3 SPI interfaces
  - CAN interface (2.0B active)
  - USB 2.0 Full speed interface (optional internal 1.5K pull-up resistor)
- Hardware encryption algorithm unit
  - Built-in hardware algorithm (DES、AES、SHA、SM1、SM3、SM4、SM7)
  - Provides a complete library of high-performance algorithms
- TRNG: The TRNG unit is used to generate a sequence of truly random numbers
  - Four independent true random sources, configurable individually
  - 128BIT random numbers can be generated at a time
  - Optional post-digital processing function
  - Attack detection
- SENSOR: Voltage and temperature sensor alarm
  - VBAT and VDD voltages can be detected separately
  - Temperature sensor available
  - Optionally reset or interrupt after alarm
- SRAM scrambling
  - Supports address and data scrambling
- One-time Programmable (OTP)
  - Support 32 Byte

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catalogue

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1 Introduction

The contents of the data manual include: the basic configuration of the product (such as the capacity of built-in Flash and RAM, the type and number of peripheral modules, etc.), the number and distribution of pins, electrical characteristics, package information, and order codes.

2 Specification

List of devices

Table 1 Device function configuration table

series		MH2103C	
Model number		CBT6	CCT6
Flash (K bytes)		128	256
SRAM(K bytes)		32	64
timer	advanced	1	1
	Be common	4	4
	basic	2	2
Communication interface	SPI	3	3
	I2C	2	2
	USART/UART	3	3
	USB	1	1
	CAN	1	1
GPIO port		37	37
12-bit ADC module (number of channels)		2(10 channels)	2(10 channels)
12-bit DAC module (number of channels)		2(2 channels)	2(2 channels)
Random number module		support	
Hardware encryption algorithm unit		support	
Page Size (K bytes)		1	2
CPU frequency		216M	
Operating voltage		2.0~3.6V	
Operating temperature		-40 to +85℃	
Encapsulation form		LQFP48	

Summarize

2.1.1 32-bit Arm® Cortex®-M3 Core with built-in flash memory and SRAM

32-bit Arm® Cortex®-The M3Core provides a low-cost platform, reduced pin count, and reduced system power consumption for the needs of the MCU, while providing superior computing performance and advanced interrupt system response.

2.1.2 Built-in flash memory

Built-in flash memory for storing programs and data.

Table 2 Matching relationship between power supply voltage and FlashDelay level

Flash Delay level	HCLK(MHz)

	Voltage Range 2.3V - 3.6V	Voltage Range 2.0V - 2.3V
0	0 < HCLK <= 108	0 < HCLK <= 32
1	108 < HCLK <= 216	32 < HCLK <= 64
2	-	64 < HCLK <= 128
3	-	128 < HCLK <= 192
4	-	192 < HCLK <= 216

2.1.3 Memory Protection Unit (MPU)

A memory protection unit (MPU) is used to manage the CPU's access to memory, preventing one task from accidentally damaging memory or resources used by another active task. This storage area is organized into up to 8 protected areas, which can be further divided into up to 8 subareas in turn. The protected area size can range from 32 bytes to the entire 4 gigabytes of addressable memory.

MPU is especially useful if there is some critical or certified code in the application that must be protected from the misbehavior of other tasks. It is usually managed by an RTOS(Real-Time Operating System). If a program accesses a memory location that is prohibited by the MPU, the RTOS detects it and takes action. In an RTOS environment, the kernel can dynamically update the MPU area Settings based on the process being executed.

2.1.4 Built-in SRAM Built-in flash memory

Up to 64K bytes of built-in SRAM, the CPU can be accessed with 0 wait cycles (read/write).

2.1.5 CRC(Cyclic redundancy Check) computing unit

CRC(Cyclic redundancy check) cells use a fixed polynomial (multiple modes optional and hardware data processing) generator to generate a CRC code from a 32-bit data word.

In many applications, CRC-based technologies are used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC60335-1 standard, it provides a means of detecting errors in flash memory.

2.1.6 Nested Vector Interrupt Controller (NVIC)

Built-in nested vector interrupt controller capable of handling up to 71 maskable interrupt channels (not including 16 Core interrupts) and 8 priorities.

- The tightly coupled NVIC enables low latency interrupt response processing
- The interrupt vector entry address goes directly to the kernel
- Tightly coupled NVIC interface
- Allows for early processing of interrupts
- Handle higher-priority interrupts that arrive late

- Supports the interrupt tail link function
- Automatically saves processor state
- Automatically resumes upon interrupt return with no additional instruction overhead

The module provides flexible interrupt management with minimal interrupt latency.

2.1.7 External Interrupt/Event Controller (EXTI)

The External Interrupt/Event controller contains 19 edge detectors for generating interrupt/event requests. Each interrupt can be configured independently with its trigger events (rising or falling edge or double edge) and can be shielded individually; There is a pending register that maintains the status of all interrupt requests. EXTI can detect clock cycles with a pulse width smaller than the internal APB2.

2.1.8 Clock and start

The selection of the system clock is made at startup, when the internal 8MHz RC oscillator is selected as the default CPU clock, and then an external 4 to 16MHz clock with failure monitoring can be selected. When an external clock failure is detected, it is isolated and the system automatically switches to the internal RC oscillator. If an interrupt is enabled, the software can receive the corresponding interrupt. Also, complete interrupt management of the PLL clock can be implemented when needed (such as when an external oscillator used indirectly fails).

Multiple pre-dividers are used to configure the frequency, high speed APB(APB2) and low speed APB(APB1) regions of the AHB. The maximum frequency of AHB and high speed APB is 216MHz, and the maximum frequency of low speed APB is 108MHz.

2.1.9 Startup mode

At startup, one of three bootstrap modes can be selected through the bootstrap pin:

- Bootstrap from program flash memory
- Bootstrap from system memory
- Bootstrap from internal SRAM

The Bootloader is stored in the system memory and can be reprogrammed via USART1.

2.1.10 Power supply scheme

- VDD: Power the I/O pins and internal regulator.
- VSSA, VDDA: Provides power to the ADC, reset module, RC oscillator, and the analog portion of the PLL. VDDA and VSSA must be connected to VDD and VSS, respectively.
- VBAT: When the VDD is turned off, power the RTC, the external 32kHz oscillator , and the backup register (via the internal power switcher). Note: All voltage ranges refer to general operating conditions.

2.1.11 Power supply monitor

A power on reset (POR)/ Power off reset (PDR) circuit is integrated inside the product, which is always in the working state to ensure that the system is on supply Work when the electricity exceeds 2V; When the VDD is below the set threshold (VPOR/PDR) , the device is placed in the reset state without the need to use an external reset circuit.

There is also a programmable voltage monitor (PVD) in the device, which monitors the VDD supply and compares it to the threshold VPVD when the VDD is below or above the threshold When an interrupt is generated during VPVD, the interrupt handler can issue a warning message or shift the microcontroller into safe mode. The PVD function needs to be enabled through a program.

2.1.12 Voltage regulator

The regulator has three operating modes: Main mode (MR), Low Power mode (LPR) and Off mode

- The main mode (MR) is used for normal operational operations
- Low Power Mode (LPR) Downtime mode for the CPU
- Shutdown mode Standby mode for the CPU: the voltage regulator output is in a high resistance state, the power supply of the core circuit is cut off, and the voltage regulator is in a zero consumption state (but the contents of the registers and SRAM are lost).

The regulator is always in operation after reset and is turned off in standby mode with high resistance output.

2.1.13 Low power mode

- Sleep pattern

In sleep mode, only the CPU stops, all peripherals are working and can wake up the CPU in the event of an interruption/event.

- Stop mode

The downtime mode allows for minimal power consumption while keeping SRAM and register contents intact. In shutdown mode, power supply to all internal 1.1V sections is stopped, the PLL, HSI RC oscillators and HSE crystal oscillators are turned off, and the regulator can be placed in normal or low power mode. The microcontroller can be awakened from shutdown mode by any signal configured as EXTI, which can be one of the 16 external I/O ports, the output of PVD, the RTC alarm clock, or the wake signal of USB.

- Standby mode

Minimum power consumption is achieved in standby mode. The internal voltage regulator is turned off, so the power supply to all internal 1.1V sections is cut off; PLL, HSI RC oscillator and HSE crystal oscillator are also turned off; After entering standby mode, the contents of the SRAM and register will disappear, but the contents of the backup register will remain, and the standby circuit will still work. The conditions for exiting from standby mode are an external reset signal on the NRST, an IWDG reset, a rising edge on the WKUP pin, or an alarm clock on the RTC.

Note: RTC, IWDG, and the corresponding clock are not stopped when entering shutdown or standby mode.

2.1.14 DMA

Supports up to 12 universal DMA channels (7 channels for DMA1 and 5 channels for DMA2) to manage memory-to-memory, device-to-memory, and memory-to-device data transfers; The DMA controller supports the management of the ring buffer, which avoids the interruption when the controller transmission reaches the end of the buffer.

Each channel has its own hardware DMA request logic, and each channel can be triggered by software. The length of the transmission, the source address of the transmission, and the destination address can be set separately through the software.

2.1.15 RTC(Real-time clock) and backup register

The RTC and the backup register are powered by a switch that selects VDD when VDD is active, otherwise it is powered by the VBAT pin. The backup registers (42 16-bit registers) can be used to hold 84 bytes of user application data when VDD is turned off. RTC and back-up registers are not reset by the system or power reset source; When awakened from standby mode, it will not be reset.3

The real-time clock has a set of continuously running counters that can provide a calendar clock function with appropriate software, and also has alarm interrupt and phased interrupt functions. The RTC's drive clock can be a 32.768kHz oscillator using an external crystal, an internal low-power RC oscillator, or a high-speed external clock with a 128 split frequency. The typical frequency of an internal low-power RC oscillator is 40kHz. To compensate for the deviation of the natural crystals, the RTC's clock can be calibrated by outputting a 512Hz signal. The RTC has a 32-bit programmable counter that allows long time measurements to be made using comparison registers. There is a 20-bit pre-divider for the timebase clock, which produces a 1-second long time reference when the clock is 32.768kHz by default.

2.1.16 Timer and watchdog

This series includes up to 1 advanced control timer, 4 normal timers, 2 basic timers , 2 watchdog timers and 1 system tick timer.

The following table compares the functions of advanced control timers, ordinary timers, and basic timers:

Table 3TIM configuration table

timer	Counter resolution	Counter type	Predivision coefficient	Generate DMA request	Capture/compare channels	Complementary output
TIM1	16-bit	Up, down, Up/down	It is an integer ranging from 1 to 65536	can	4	yes
TIM2 TIM3 TIM4 TIM5	16-bit	Up, down, Up/down	It is an integer ranging from 1 to 65536	can	4	none
TIM6 TIM7	16-bit	Make progress	It is an integer ranging from 1 to 65536	can	0	none

Advanced Control Timer (TIM1)

The two advanced control timers (TIM1) can be thought of as three-phase PWM generators assigned to 6 channels, with complementary PWM outputs with dead-time insertion, and as complete universal timers. Four separate channels can be used for:

- Input capture
- Output comparison
- Generate PWM(edge or center alignment mode)
- Single pulse output

When configured as a 16-bit standard timer, it has the same functionality as the TIMx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0 to 100%).

In debug mode, the counter can be frozen while the PWM outputs are disabled, thus cutting off the switches controlled by these outputs. Many of the functions are the same as standard TIM timers, and the internal structure is the same, so advanced control timers can operate in conjunction with TIM timers through the timer link function to provide synchronization or event link functions.

Universal timer (TIM2, TIM3, TIM4, TIM5)

In this series, there are 4 standard timers (TIM2, TIM3, TIM4, TIM5) that can run synchronously. Each timer has a 16-bit auto-load tapered/decrement counter, a 16-bit pre-divider, and four separate channels, each for input capture, output comparison, PWM and monopulse mode output. They can also work with advanced control timers via the timer link function to provide synchronization or event link functionality. In debug mode, counters can be frozen. Any standard timer can be used to generate PWM output. Each timer has its own DMA request mechanism.

These timers are also capable of processing signals from incremental encoders, as well as digital outputs from one to three Hall sensors.

Independent watchdog

The independent watchdog is based on a 12-bit decrement counter and an 8-bit pre-divider, which is clocked by an internally independent 40kHz RC oscillator; Because the RC oscillator is independent of the master clock, it can operate in both down and standby modes. It can be used as a watchdog to reset the entire system in the event of a problem, or as a free timer to provide time-out management for applications. Option bytes can be configured to be software or hardware enabled watchdog. In debug mode, counters can be frozen.

Basic timers TIM6 and TIM7

These timers are mainly used for the generation of DAC triggers. They can also be used as a universal 16-bit time base.

Window guard dog

The window watchdog has a 7-bit decrement counter and can be set to run freely. It can be used as a watchdog to reset the entire system in case of problems. It is driven by the master clock and has the function of early warning interruption; In debug mode, counters can be frozen.

System time base timer

This timer is designed for real-time operating systems and can also be used as a standard decrement counter. It has the following characteristics:

- 24-bit decrement counter
- Automatic reloading function
- Generates a maskable system interrupt when the counter is 0
- Programmable clock source

2.1.17 I2C bus

Up to 2 I2C bus interfaces, capable of working in multi-master or slave mode, supporting standard and fast modes. The I2C interface supports 7-bit or 10-bit addressing, and dual-slave addressing in 7-bit slave mode. Built-in hardware CRC generator/verifier.

They can operate using DMA and support SMBus version 2.0 /PMBus.

2.1.18 Universal Synchronous/Asynchronous Transceiver (USART)

Three universal synchronous/asynchronous transceivers (USART1, USART2 and USART3). These three interfaces provide asynchronous communication, IrDASIRENDEC, multiprocessor communication mode, single-wire half-duplex communication mode, and LIN master/slave functionality.

USART1, USART2, and USART3 interfaces feature hardware CTS and RTS signal management, ISO7816-compatible smart card mode, and SPI-like communication mode.

2.1.19 Serial Peripheral Interface (SPI)

Up to 3 SPI interfaces. The 3-bit pre-divider produces 8 master mode frequencies that can be configured to be 8 or 16 bits per frame. Hardware CRC generation/ verification supports basic SD card and MMC modes. All SPI interfaces can use DMA operations.

2.1.20 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B(active) with bit rates up to 1 megabit/SEC. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers. It has 3 sending mailboxes and 2 receiving FIFOs, 3 stages and 14 adjustable filters.

2.1.21 Universal Serial Bus (USB)

A built-in full-speed USB-compatible device controller follows the full-speed USB device (12 megabits/SEC) standard, and the endpoint can be configured by software with standby/wake function. The USB-specific 48MHz clock is generated directly from the internal master PLL (clock source is optional).

2.1.22 Universal Input/Output Interface (GPIO)

Each GPIO pin can be configured by software to be an output (push-pull or leak-open) , an input (with or without pull or drop down), or a reusable peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals. With the exception of ports with analog input functions, all GPIO pins have high current flow capability.

In case of need, the peripheral function of the I/O pin can be locked with a specific operation to avoid accidental writing to the I/O register. Each I/O can be configured with forced up and down resistors to save external resistance consumption.

2.1.23 ADC(Analog/Digital Converter)

Supports up to 2 12-bit analog/digital converters (ADCs) with up to 10 external channels for single or scan conversion. In scan mode, the conversion on a selected set of analog inputs is automatically performed.

Additional logic functions on the ADC interface include:

- Synchronous sampling and holding
- Cross sampling and holding
- Single sampling

An ADC can operate using DMA.

The analog watchdog feature allows very precise monitoring of one, multiple, or all selected channels, resulting in an interruption when the monitored signal exceeds a preset threshold.

Events generated by standard timers and advanced control timers can be internally cascaded to the ADC start trigger and injection trigger, respectively, and the application can synchronize the AD transition with the clock.

2.1.24 DAC(Digital/Analog Signal Converter)

Two 12-bit buffered DAC channels can be used to convert a 2-channel digital signal into a 2-channel analog voltage signal and output it.

This dual digital interface supports the following functions:

- Two DAC converters: one output channel each 8-bit or 12-
- bit monotonic output
- Align left and right data in 12-bit mode
- Synchronous update function
- Generating noise wave
- Triangular wave generation
- Dual DAC channel independent or synchronous conversion
- DMA capabilities are available for each channel
- External trigger for conversion
- Input reference voltage V REF+

The DAC channel can be triggered by the update output of the timer, and the update output can also be connected to different DMA channels.

2.1.25 Temperature sensor

The temperature sensor produces a voltage that varies linearly with temperature. The temperature sensor is internally connected to the input channel of the ADC1_IN16 for converting the output of the sensor into a numeric value.

2.1.26 Serial Single-wire JTAG Debugging Port (SWJ-DP)

Embedded SWJ-DP interface, which is a combination of JTAG and serial single-line debugging interface, can achieve serial single-line debugging interface or JTAG interface connection. JTAG's TMS and TCK signals share pins with SWDIO and SWCLK, respectively, and a special signal sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.1.27 Embedded Tracking Module (ETM)

The use of embedded Trace microunits (ETM) connected to external Trace port analysis (TPA) devices with few ETM pins outputs compressed data streams at high speeds from the CPU core, providing developers with clear information on instruction running and data flow. The TPA device can be connected to the debugging host through USB, Ethernet or other high-speed channels, and the real-time instruction and data flow can be recorded by the debugging software on the debugging host and displayed in the required format. TPA hardware can be purchased from development tool vendors and is compatible with third-party debugging software.

2.1.28 True Random Number Generator (TRNG)

TRNG units are used to generate sequences of truly random numbers. A sequence of 128-bit truly random numbers is generated at a time. The CPU interrupt request can be generated after the random number is generated.

3 Pin definition

LQFP48 package

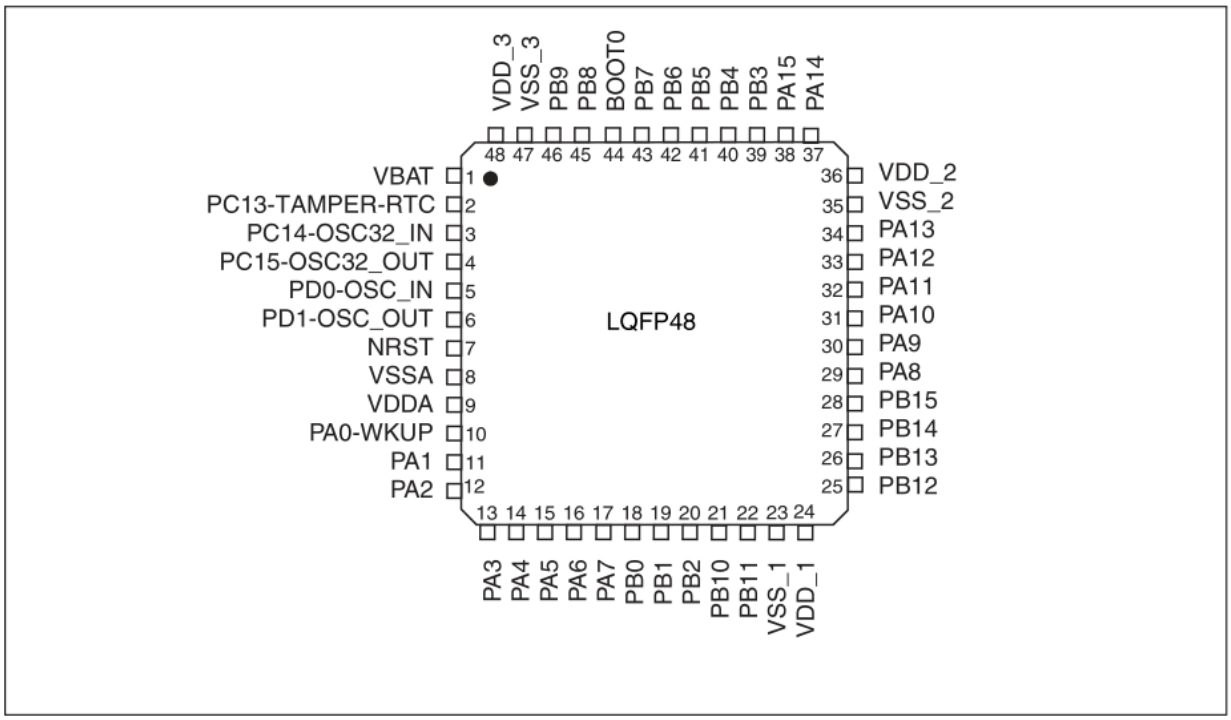


Figure 1LQFP48 package

LQFP48 Pin definition

Table 4LQFP 48 Pin definition configuration table

LQFP 48	Pin Name	Type	I/O Level	Main Function (after reset)	Default	Remap
1	VBAT	S	-	VBAT	-	-
2	PC13-TAMPERRTC	I/O	-	PC13	TAMPER-RTC	-
3	PC14-OSC32_IN	I/O	-	PC14	OSC32_IN	-
4	PC15-OSC32_OUT	I/O	-	PC15	OSC32_OUT	-
5	OSC_IN	I/O	-	OSC_IN	-	PD0
6	OSC_OUT	I/O	-	OSC_OUT	-	PD1
7	NRST	I/O	-	NRST	-	-
8	VSSA	S	-	VSSA	-	-
9	VDDA	S	-	VDDA	-	-
10	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS/ ADC12_IN0/TIM2_CH1_ETR/ TIM5_CH1	-
11	PA1	I/O	-	PA1	USART2_RTS/ADC12_IN1/ TIM2_CH2/TIM5_CH2	-
12	PA2	I/O	-	PA2	USART2_TX/ADC12_IN2/ TIM2_CH3/TIM5_CH3/	-
13	PA3	I/O	-	PA3	USART2_RX/ADC12_IN3/ TIM2_CH4/TIM5_CH4/	-

14	PA4	I/O	-	PA4	SPI1_NSS/USART2_CK/ DAC_OUT1/ADC12_IN4	-
15	PA5	I/O	-	PA5	SPI1_SCK/ADC12_IN5/ DAC_OUT2	-
16	PA6	I/O	-	PA6	SPI1_MISO/ADC12_IN6/ TIM3_CH1	TIM1_BKIN
17	PA7	I/O	-	PA7	SPI1_MOSI/ADC12_IN7/ TIM3_CH2	TIM1_CH1N
18	PB0	I/O	-	PB0	ADC12_IN8/TIM3_CH3	TIM1_CH2N
19	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4	TIM1_CH3N
20	PB2	I/O	FT	PB2/BOOT1	-	-
21	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX	TIM2_CH3
22	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX	TIM2_CH4
23	VSS_1	S	-	VSS_1	-	-
24	VDD_1	S	-	VDD_1	-	-
25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/ USART3_CK/TIM1_BKIN	-
26	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS/ TIM1_CH1N	-
27	PB14	I/O	FT	PB14	SPI2_MISO/USART3_RTS/ TIM1_CH2N	-
28	PB15	I/O	FT	PB15	SPI2_MOSI/TIM1_CH3N	-
29	PA8	I/O	FT	PA8	USART1_CK/TIM1_CH1/ MCO	-
30	PA9	I/O	FT	PA9	USART1_TX/TIM1_CH2	-
31	PA10	I/O	FT	PA10	USART1_RX/TIM1_CH3	-
32	PA11	I/O	-	PA11	USART1_CTS/USBDM CAN_RX/TIM1_CH4	-
33	PA12	I/O	-	PA12	USART1_RTS/USBDP/ CAN_TX/TIM1_ETR	-
34	PA13	I/O	FT	JTMS-SWDIO	-	PA13
35	VSS_2	S	-	VSS_2	-	-
36	VDD_2	S	-	VDD_2	-	-
37	PA14	I/O	FT	JTCK-SWCLK	-	PA14
38	PA15	I/O	FT	JTDI	SPI3_NSS	TIM2_CH1_ETR/PA15/ SPI1_NSS
39	PB3	I/O	FT	JTDO	SPI3_SCK	TIM2_CH2/PB3/ TRACESWO/SPI1_SCK
40	PB4	I/O	FT	NJTRST	SPI3_MISO	TIM3_CH1/PB4/ SPI1_MISO
41	PB5	I/O	-	PB5	I2C1_SMBA/ SPI3_MOSI	TIM3_CH2/SPI1_MOSI
42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2	USART1_RX
44	BOOT0	I	-	BOOT0	-	-
45	PB8	I/O	FT	PB8	TIM4_CH3	I2C1_SCL/CAN_RX
46	PB9	I/O	FT	PB9	TIM4_CH4	I2C1_SDA/CAN_TX
47	VSS_3	S	-	VSS_3	-	-
48	VDD_3	S	-	VDD_3	-	-

(1)FT =5V tolerance

4 Electrical characteristic

Test condition

Unless otherwise specified, all voltages are VSS based.

4.1.1 Minimum and maximum values

Unless otherwise specified, all minimum and maximum values are guaranteed under the worst conditions of ambient temperature, supply voltage and clock frequency on the production line by testing 100% of the product at ambient temperature TA=25 ° C.

Note below each table that data obtained through comprehensive evaluation, design simulation and/or process characteristics will not be tested on the production line; On the basis of comprehensive evaluation, the minimum and maximum values are obtained by taking the average value of the sample test and adding or subtracting three times the standard distribution (average ±3Σ).

4.1.2 Typical value

Unless otherwise noted, typical data are based on TA=25 ° C and VDD=3.3V. These data are for design guidance only and are not tested.

Typical ADC accuracy values are obtained by sampling a standard batch and testing at all temperature ranges, and 95% of products have an error of less than or equal to the given value (mean ±2Σ).

4.1.3 Typical curve

Unless otherwise noted, typical curves are intended as a design guide only and are not tested.

4.1.4 Load capacitance

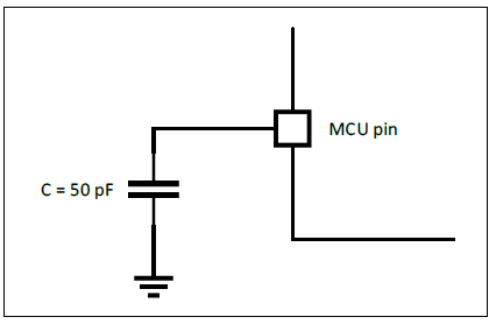


Figure 2 Load conditions for the pins

4.1.5 Pin input voltage

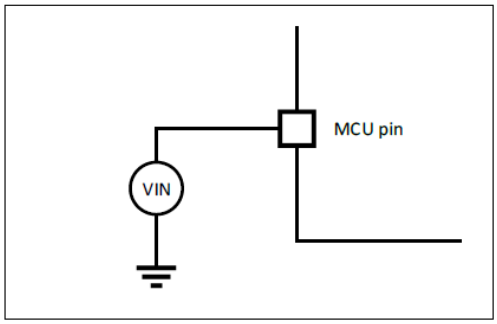


Figure 3 Pin input voltage

4.1.6 Power supply scheme

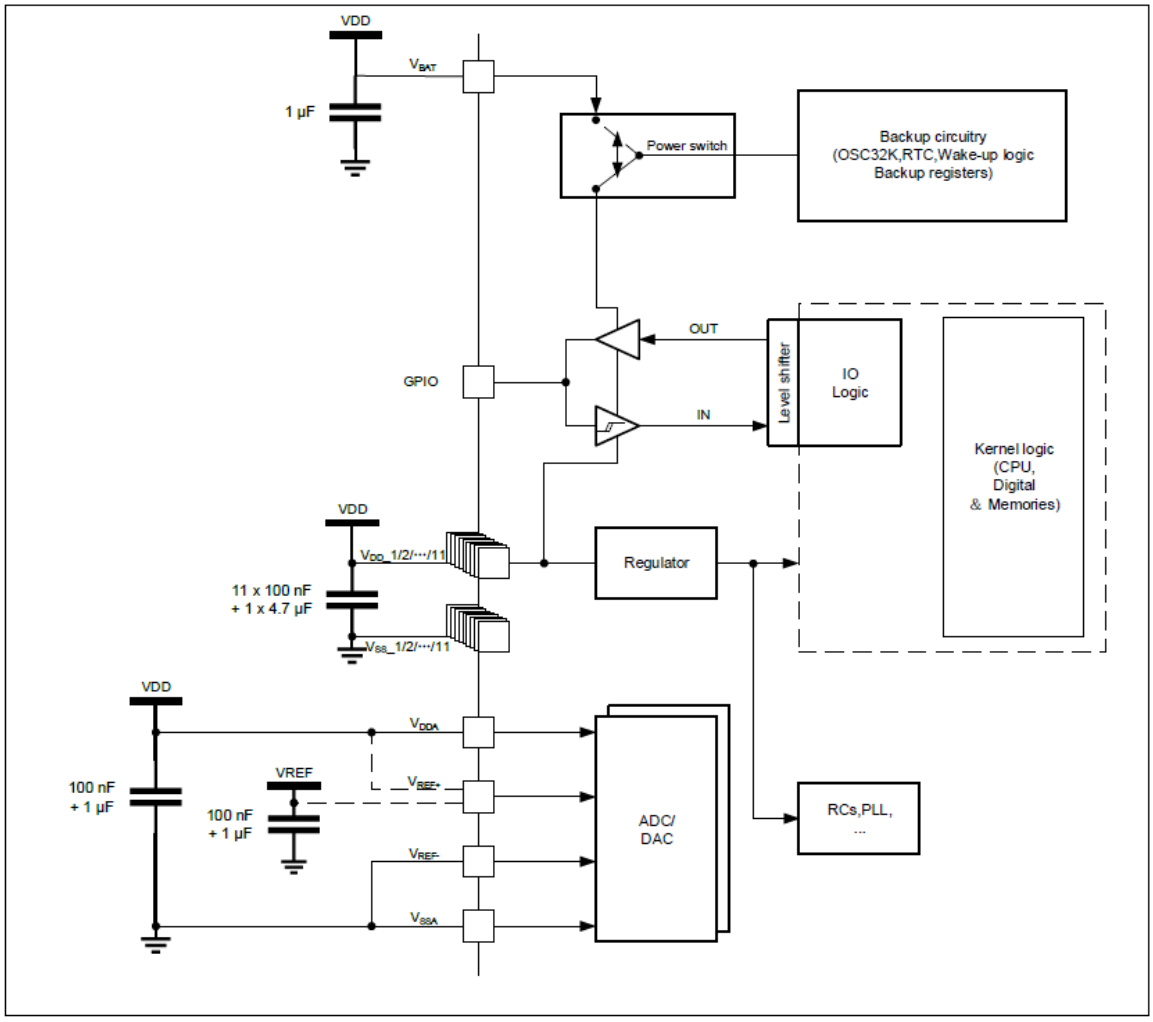


Figure 4 Power supply scheme

4.1.7 Current consumption measurement

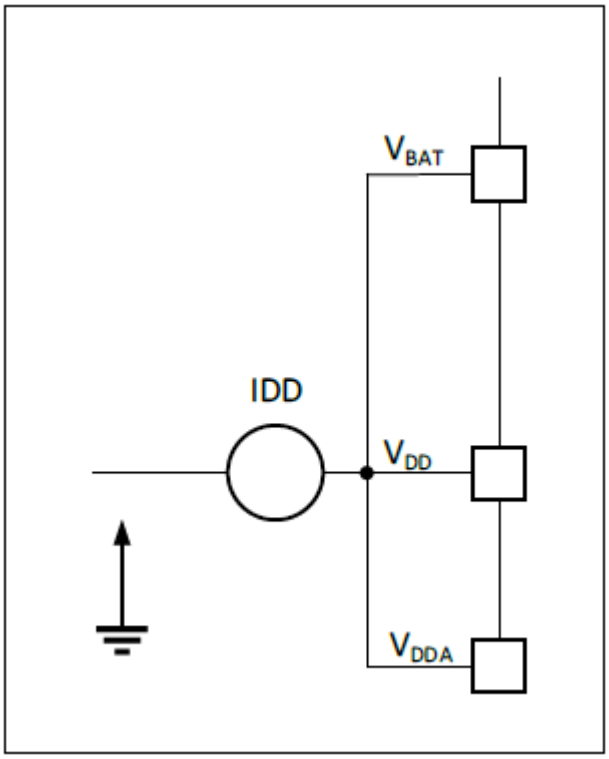


Figure 5 Current consumption measurement scheme

Absolute maximum rating

A load applied to the device that exceeds the value given in the Absolute Maximum Rating list may cause the device to be permanently damaged. Only the maximum load that can be borne is given here, and it does not mean that the functional operation of the device under these conditions is correct. The reliability of the device will be affected if the device works at the maximum value for a long time.

Table 5 Voltage characteristics

symbol	Description	Minimum value	Maximum value	unit
VDD - VSS	External main supply voltage (including VDDA and VDD)(1)	-0.3	4	V
VIN	Input voltage on 5V tolerant pins (2)	Vss-0.3	Vdd+4.0	
	Input voltage on other pins (2)	Vss-0.3	4.0	
|ΔVDDx|	Voltage difference between different supply pins	—	50	mV
|VSSx-VSS|	Voltage difference between different ground pins	—	50	

(1) All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply system within the allowable range.

(2) Contains VREF-feet.

Table 6 Current characteristics

symbol	Description	Maximum value (1)	unit
IVDD	Total current through the VDD/VDDA power line (supply current) (1)	150	mA
IVSS	Total current through the VSS ground wire (outflow current) (1)	150	
IIO	Output feed current on any I/O and control pin	25	
	Output current on any I/O and control pin	-25	

(1) All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply system within the allowable range.

Table 7 Temperature characteristics

symbol	Description	Numerical value	unit
TSTG	Storage temperature range	-65 ~ +150	℃
TJ	Maximum junction temperature	105	℃

Working condition

4.1.8 General operating conditions

Table 8 General working conditions

symbol	argument	Conditions	Minimum value	Maximum value	unit
fHCLK	Internal AHB clock frequency	—	0	216	MHz
fPCLK1	Internal APB1 clock frequency	—	0	108	
fPCLK2	Internal APB2 clock frequency	—	0	216	
VDD	Standard operating voltage	—	2.0	3.6	V
VDDA(1)	Simulate part of the operating voltage	Must be the same as VDD	2.0	3.6	V
VBAT	Backup part of the operating voltage		1.6	3.6	V
TA	Ambient temperature	—	-40	85	℃

(1) It is recommended to use the same power supply for VDD and VDDA.

4.1.9 Working conditions during power-on and power-off

The parameters given in the following table are based on ambient temperatures listed in the general operating conditions.

Table 9 Operating conditions for power-on and power-off

symbol	argument	Conditions	Minimum value	Maximum value	unit
tVDD	VDD rising rate	—	0	∞	us/V
	VDD decline rate		20	∞	

4.1.10 Built-in reset and power control module features

The parameters given in the following table are tested at VDD supply voltages listed under common operating conditions.

Table 10 Built-in reset and power control module characteristics

symbol	argument	Conditions	Minimum value	Typical value	Maximum value	unit
VPVD	Programmable voltage detector for level selection	PLS[2:0]=000 (rising edge)	2.18	2.22	2.25	V
		PLS[2:0]=000 (falling edge)	2.08	2.14	2.20	V
		PLS[2:0]=001 (rising edge)	2.28	2.32	2.35	V
		PLS[2:0]=001 (falling edge)	2.18	2.24	2.30	V
		PLS[2:0]=010 (rising edge)	2.38	2.42	2.45	V
		PLS[2:0]=010 (falling edge)	2.28	2.34	2.40	V
		PLS[2:0]=011 (rising edge)	2.48	2.52	2.55	V

		PLS[2:0]=011 (falling edge)	2.38	2.44	2.50	V
		PLS[2:0]=100 (rising edge)	2.58	2.62	2.65	V
		PLS[2:0]=100 (falling edge)	2.48	2.54	2.60	V
		PLS[2:0]=101 (rising edge)	2.68	2.72	2.75	V
		PLS[2:0]=101 (falling edge)	2.58	2.64	2.70	V
		PLS[2:0]=110 (rising edge)	2.78	2.82	2.85	V
		PLS[2:0]=110 (falling edge)	2.68	2.74	2.80	V
		PLS[2:0]=111 (rising edge)	2.88	2.94	2.95	V
		PLS[2:0]=111 (falling edge)	2.78	2.84	2.90	V
VPVDhyst(1)	PVD hysteresis	—	—	80	—	mV
VPOR/PDR	Power-on/power-off reset threshold	Falling edge	—	1.97	—	V
		Rising edge	—	2.02	—	V
VPDRhyst(1)	PDR hysteresis	—	—	50	—	mV
TRSTTEMPO(1)	Reset duration	—	—	2	—	ms

(1) Guaranteed by design, not tested in production.

4.1.11 Built-in reference voltage

The parameters given in the following table are tested at VDD supply voltages listed under common operating conditions.

Table 11 Built-in reference voltage

symbol	argument	Conditions	Minimum value	Typical value	Maximum value	unit
VREFINT	Built-in reference voltage	-40℃ < TA < +85℃	1.16	1.20	1.24	V
TS_vrefint(1)	When reading internal parameters At voltage, ADC Sampling time of	—	-	5.1	17.1	us
TCoeff(2)	Temperature coefficient	—	—	—	100	ppm/℃

(1) The shortest sampling time is obtained through multiple cycles in the application.

(2) Guaranteed by design, not tested in production.

4.1.12 Supply current characteristic

Current consumption is a comprehensive indicator of a variety of parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin turnover rate, program location in memory, and code execution.

For the measurement method of current consumption, see the description of current consumption measurement in the section of Test Conditions.

Current consumption

The microcontroller is under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are turned off unless otherwise specified.
- When turning on peripherals:fPCLK1 = fHCLK/2, fPCLK2 = fHCLK。

Table 12 Current consumption in operating mode

symbol	argument	Conditions	fHCLK	Typical values (1)		Maximum value (2)		unit
				Enable all peripherals	Turn off all peripherals	Enable all peripherals	Turn off all peripherals	
IDD	Supply current in operating mode	External clock (3)	216MHz	36.29	25.49	38.50	27.56	mA
			168MHz	27.71	19.27	29.95	21.35	
			72MHz	13.09	9.38	14.93	11.21	
			48MHz	9.35	6.93	11.18	8.74	
			32MHz	6.88	5.25	8.68	7.04	
			24MHz	5.67	4.46	7.41	6.20	
			16MHz	4.43	3.63	6.16	5.34	
			8MHz	3.28	2.58	4.98	4.54	
		Running at high speed internal RC oscillator (HSI)	128MHz	21.64	15.19	23.89	17.27	mA
			72MHz	13.03	9.39	15.03	11.31	
			48MHz	9.34	6.92	11.26	8.78	
			32MHz	7.55	5.73	8.73	7.08	
			24MHz	5.69	4.49	7.74	6.24	
			16MHz	4.45	3.66	6.21	5.39	
			8MHz	3.30	2.88	5.02	4.57	

(1) The typical value is obtained when TA=25℃ and VDD=3.3V.

(2) The maximum value is measured at TA=85℃ and VDD=3.6V.

(3) The external clock is 8MHz, and PLL is enabled when fHCLK>8MHz.

Table 13 Current consumption in sleep mode, code running in Flash

symbol	argument	Conditions	fHCLK	Typical values (1)		Maximum value (2)		unit
				Enable all peripherals	Turn off all peripherals	Enable all peripherals	Turn off all peripherals	
IDD	Supply current in sleep mode	External clock (3)	216MHz	25.72	7.01	27.73	8.70	mA
			168MHz	19.46	4.81	21.49	6.58	
			72MHz	9.53	3.25	11.31	4.92	
			48MHz	6.99	2.81	8.76	4.51	
			32MHz	5.32	2.54	7.07	4.23	
			24MHz	4.50	2.41	6.22	4.09	
			16MHz	3.66	2.28	5.36	3.96	
			8MHz	2.90	2.17	4.57	3.84	
		Runs on a high speed internal RC oscillator (HSI)	128MHz	15.31	4.14	17.36	5.90	mA
			72MHz	9.47	3.20	11.36	4.93	
			48MHz	6.97	2.80	8.80	4.52	
			32MHz	5.32	2.54	7.11	4.26	
			24MHz	4.49	2.41	6.25	4.12	
			16MHz	3.65	2.27	5.39	3.98	
			8MHz	2.89	2.17	4.61	3.87	

(1) The typical value is obtained when TA=25℃ and VDD=3.3V.

(2) The maximum value is measured at TA=85℃ and VDD=3.6V.

(3) The external clock is 8MHz, and PLL is enabled when fHCLK>8MHz.

Table 14 Typical and maximum current consumption in down and standby modes

symbol	argument	Conditions	Typical values (1)	Maximum value (2)	unit

IDD	Supply current in shutdown mode	The regulator is in operation mode at low and high speed internal RC oscillators and external high speed oscillators In closed state (no independent watchdog)	160	1100	uA
		The regulator is in low power mode, low speed, high speed internal RC oscillator and external high speed oscillator Closed (no independent watchdog)	120	1000	
	Supply current in standby mode	The low speed internal RC oscillator, the external low speed oscillator and the RTC and IWDG are turned off	0.7	2.2	
		The low speed internal RC oscillator is on, and the external low speed oscillator and RTC and IWDG are off	1.0	2.5	
		The external low-speed oscillator is on, and the low-speed internal RC oscillator and RTC and IWDG are off Closed state	1.0	2.6	
		The external low speed oscillator and RTC are on, and the low speed internal RC oscillator and IWDG are on Off state	1.3	2.7	
		The low speed internal RC oscillator and IWDG are on, and the external low speed oscillator and RTC are on Off state	1.0	2.7	
IDD_VBAT	Supply current of the backup area	The external low speed oscillator and RTC are on	0.9	1.3	

(1) The typical value is obtained when TA=25℃ and VDD=VBAT=3.3V.

(2) The maximum value is measured at TA=85℃ and VDD=VBAT=3.6V.

(3) It is derived from comprehensive evaluation and is not tested in production.

Built-in peripheral current consumption

MCU operating conditions are as follows:

- All I/O pins are in analog input mode
- All peripherals are turned off unless otherwise specified.
- The value given is calculated by measuring current consumption
  - ◆ Turn off the clocks of all peripherals
  - ◆ Turn on only one peripheral clock

Table 15 Current consumption of built-in peripherals

Built-in peripheral		Typical power consumption at 25℃	unit
APB1	TIM2	2.08	uA/MHz
	TIM3	2.36	
	TIM4	2.22	
	TIM5	2.08	
	TIM6	0.14	
	TIM7	0.14	
	SPI2	0.97	
	SPI3	0.83	
	USART2	0.56	
	USART3	0.56	

	I2C1	1.81	
	I2C2	1.81	
	USB	5.42	
	CAN	1.11	
	WWDG	0.24	
	DAC	0.58	
	PWR	0.008	
	BKP	0.11	
APB2	ADC1(1)	5	
	ADC2(1)	5	
	TIM1	3.71	
	SPI1	1.83	
	USART1	0.56	

(1) Special conditions of ADC: fHCLK=56MHz, fAPB1=fHCLK/2, fAPB2=fHCLK, fADCCLK= FAPB1 /4, ADC_CR2

The ADON of the register =1.

4.1.13 External clock source features

High speed external user clock generated from an external oscillating source

The characteristic parameters given in the following table are measured using a high speed external clock source with ambient temperature and supply voltage conforming to common operating conditions.

Table 16 High speed external user clock characteristics

symbol	argument	Conditions	Minimum value	Typical value	Maximum value	unit
fHSE_ext	User External Clock Frequency (1)	—	0.615	8	35	MHz
VHSEH	OSC_IN Input pin high level voltage		0.48Vdd	—	Vdd	V
VHSEL	OSC_IN Input pin low voltage		Vss	—	0.38Vdd	
tw(HSE) tw(HSE)	OSC_IN high or low time (1)		5	—	—	ns
tr(HSE) tf(HSE)	Time for OSC_IN to rise or fall (1)		—	—	20	
Cin(HSE)	OSC_IN Input Tolerance (1)	—	—	5	—	pF
DuCy(HSE)	Duty cycle	—	45	50	55	%

(1) Guaranteed by design, not tested in production.

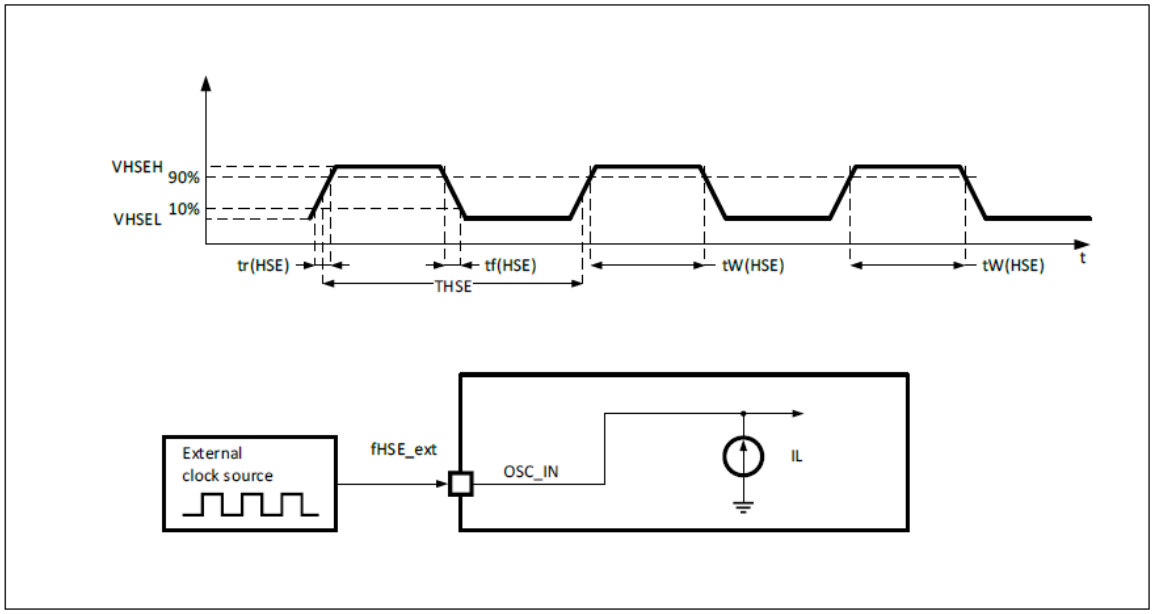


Figure 6 AC timing diagram of the external high-speed clock source

Low speed external user clock generated from an external oscillating source

The characteristic parameters given in the following table are measured using a low speed external clock source, and the ambient temperature and supply voltage meet the general operating conditions.

Table 17 Low-speed external user clock characteristics

symbol	argument	Conditions	Minimum value	Typical value	Maximum value	unit
fHSE_ext	User External Clock Frequency (1)	—	—	32.768	1000	KHz
VLSEH	OSC32_IN Input pin High level voltage	—	0.48Vdd	—	VDD	V
VLSEL	OSC32_IN Input pin low voltage	—	VSS	—	0.38Vdd	V
tw(LSE) tw(LSE)	OSC32_IN High or low duration (1)	—	450	—	—	ns
tr(LSE) tf(LSE)	OSC32_IN rise or fall time (1)	—	—	—	50	ns
Cin(LSE)	OSC32_IN Input Tolerance (1)	—	—	5	—	pF
DuCy(LSE)	Duty cycle	—	30	50	70	%

(1) Guaranteed by design, not tested in production.

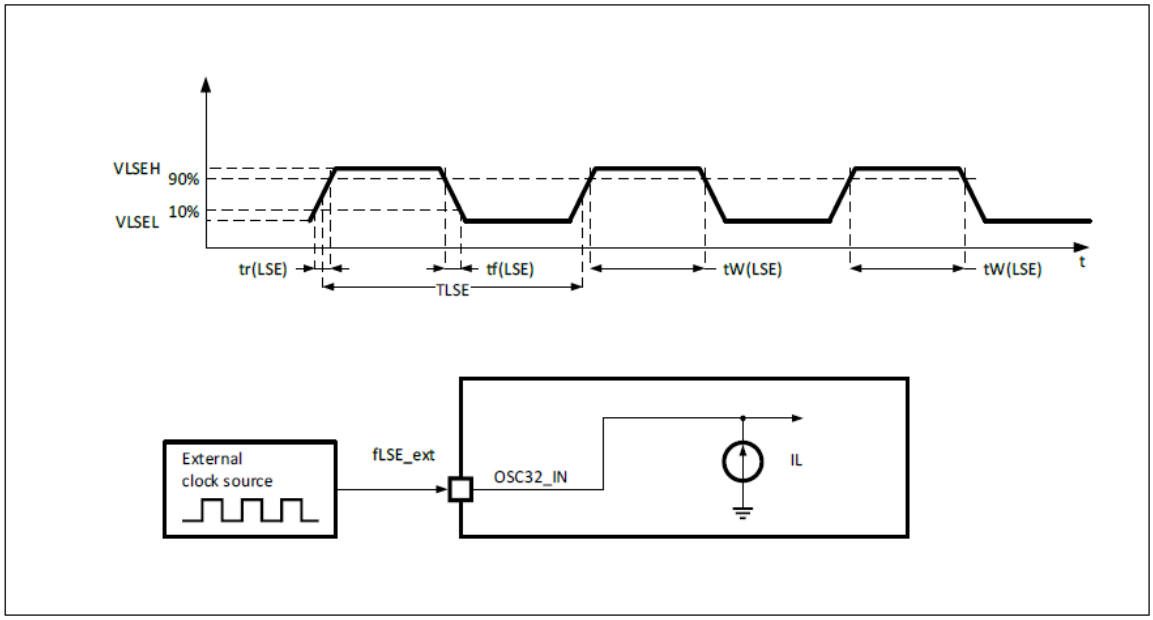


Figure 7 AC timing diagram of an external low-speed clock source

High speed external clock generated using a crystal/ceramic resonator

The high speed external clock (HSE) can be generated using an oscillator consisting of a crystal/ceramic resonator of 4 to 16MHz. The information presented in this section is based on a comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and the load capacitor must be placed as close as possible to the pin of the oscillator to reduce output distortion and the stability time at startup. For detailed parameters of the crystal resonator (frequency, package, accuracy, etc.), please consult the respective manufacturer. (Note: The crystal resonator mentioned here is what we usually say is a passive crystal oscillator)

Table 18HSE 4~16MHz oscillator characteristics (1)(2)

symbol	argument	Conditions		Minimum value	Typical value	Maximum value	unit
fOSC_IN	Oscillator frequency	—		4	8	16	MHz
tSU(HSE)	Start-up time	VDD is stable	TA = -40℃	—	790	—	us
			TA = 25 ℃	—	860	—	
			TA = 85 ℃	—	960	—	

(1) The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

(2) It is derived from comprehensive evaluation and is not tested in production.

(3)tSU(HSE) is the startup time, measured from the time the software enables HSE until a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and may vary greatly depending on the crystal manufacturer.

For CL1 and CL2, it is recommended to use a high quality ceramic capacitor between 5 pF and 25 pF designed for high frequency applications (typical value), and select a crystal or resonator that meets the requirements. Usually CL1 and CL2 have the same parameters. Crystal manufacturers usually give load capacitance parameters in a serial combination of CL1 and CL2. When selecting CL1 and CL2, the capacitive reactance of the PCB and MCU pins should be taken into account (the capacitance of the pins to the PCB can be roughly estimated at 10 pF).

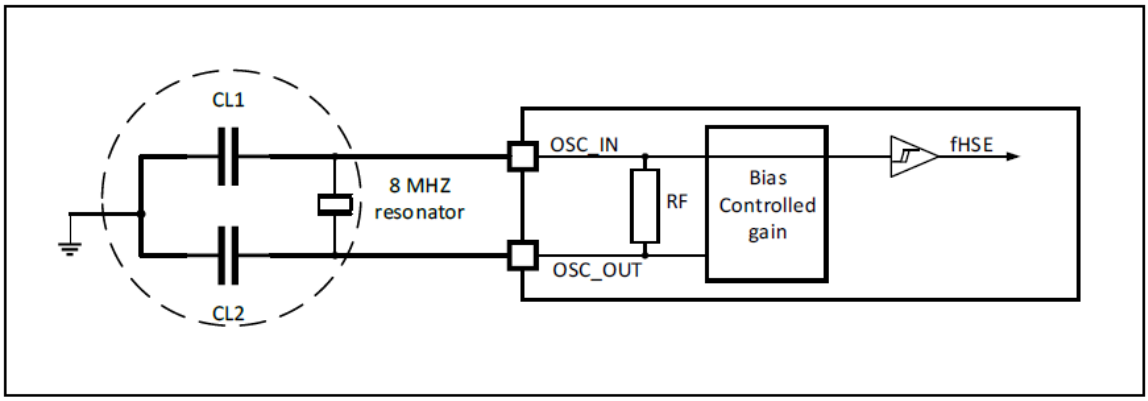


Figure 8 Typical applications using 8MHz crystals

Low speed external clock generated using a crystal/ceramic resonator

The low speed external clock (LSE) can be generated using an oscillator with a 32.768kHz crystal/ceramic resonator. The information presented in this section is the result of a comprehensive characteristic evaluation. In the application, the resonator and the load capacitor must be placed as close as possible to the pin of the oscillator to reduce output distortion and the stability time at startup. For detailed parameters of the crystal resonator (frequency, package, accuracy, etc.), please consult the respective manufacturer. (Note: The crystal resonator mentioned here is what we usually say is a passive crystal oscillator)

Table 19LSE oscillator characteristics (fLSE=32.768kHz)(1)

symbol	argument	Conditions		Minimum value	Typical value	Maximum value	unit
tSU(HSE)	Start-up time	VDD is stable	TA = -40℃	—	321	—	ms
			TA = 25 ℃	—	221	—	
			TA = 85 ℃	—	223	—	

(1) It is derived from comprehensive evaluation and is not tested in production.

For CL1 and CL2, it is recommended to use a high-quality ceramic capacitor between 5 pF and 15 pF, and select a crystal or resonator that meets the requirements. Usually CL1 and CL2 have the same parameters. Crystal manufacturers usually give load capacitance parameters in a serial combination of CL1 and CL2.

The load capacitance CL is calculated by the following formula: CL = CL1 x CL2 / (CL1 + CL2) + Cstray, where Cstray is the capacitance of the pin and the PCB board or PCB-related capacitance, and its typical value is between 2 pF and 7 pF.

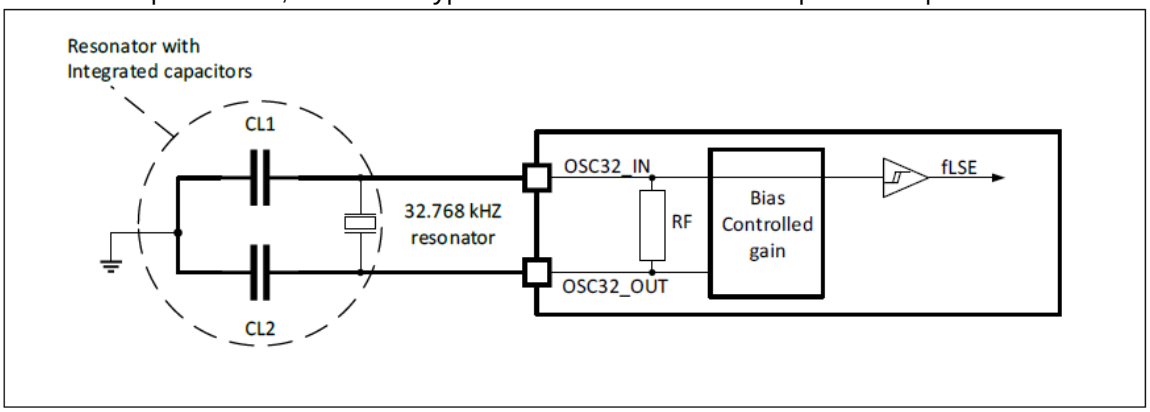


Figure 9 Typical application using a 32.768KHz crystal

4.1.14 Features of the internal clock source

The characteristic parameters given in the following table are measured using ambient temperature and supply voltage in accordance with common operating conditions.

High speed internal (HSI)RC oscillator

Table 20 HSI Oscillator Characteristics (1)

symbol	argument	Conditions	Minimum value	Typical value	Maximum value	unit
fHSI	frequency	—	—	8	—	MHz
ACCHSI	Accuracy of HSI oscillator	TA = -40~85℃	-2.5	—	3.5	%
tSU(HSI)	HSI oscillator startup time	—	—	10	—	us
IDD(HSI)	HSI oscillator power consumption	—	—	3.5	—	uA

(1) VDD = 3.3V, TA = -40~85℃, Unless otherwise stated.

Low speed internal (LSI)RC oscillator

Table 21LSI Oscillator Characteristics (1)

symbol	argument	Conditions	Minimum value	Typical value	Maximum value	unit
fLSI(2)	frequency	—	38	40	42	kHz
tSU(LSI)(3)	LSI oscillator startup time	—	—	75	—	us
IDD(LSI)(3)	LSI oscillator power consumption	—	—	0.28	—	uA

(1) VDD = 3.3V, TA = -40~85℃, unless otherwise specified.

(2) It is derived from comprehensive evaluation and is not tested in production

(3) Guaranteed by design, not tested in production

4.1.15 Time to wake up from low power mode

The wake times listed in the table below are measured during the wake phase of an 8MHz HSI RC oscillator. The clock source used for wake up depends on the current operating mode:

- Down or standby mode: The clock source is the RC oscillator
- Sleep mode: The clock source is the clock used to enter sleep mode

All times are measured using ambient temperature and supply voltage conforming to common operating conditions.

Table 22 Wake up time of low power mode

symbol	argument	Typical value	unit
tWUSLEEP(1)	Wake up from sleep mode	10	CPU clock cycle
tWUSTOP(1)	Wake up from shutdown mode (Low power mode for voltage regulator)	12	us
tWUSTDBY(1)	Wake up from standby mode	260	us

(1) The wake up time is measured from the wake up event until the user program reads the first instruction.

4.1.16 PLL characteristics

The parameters listed in the following table are measured using ambient temperature and supply voltage conforming to common operating conditions.

Table 23PLL features

symbol	argument	Numerical value			unit
		Minimum value	Typical value	Maximum value (1)	
fPLL_IN	PLL Input Clock (2)	1	8	32	MHz
	PLL Input clock duty cycle	40	—	60	%

fPLL_OUT	PLL frequency doubled output clock	4	—	216	MHz
tLOCK	PLL phase lock time	—	51.2	87.8	us
Jitter	Cyclic jitter	—	—	200	ps

(1) It is derived from comprehensive evaluation and is not tested in production.
(2) Care needs to be taken to use the correct frequency doubling factor, so that the fPLL_OUT is within the allowable range according to the PLL input clock frequency.

4.1.17 Memory characteristic

Flash memory

Unless otherwise specified, all characteristic parameters are obtained at TA = -40~85 ° C.

Table 24 Flash memory characteristics

symbol	argument	Conditions	Typical value	unit
tPROG	16 bit programming time	—	50	us
tERASE	Page erase time	—	25	ms
tME	Whole chip erase time	—	3	s

Table 25 Flash memory life and data retention life

symbol	argument	Condition	Minimum value (1)	Typical value	Maximum value	unit
NEND	Life span (Note: erase times)	TA^S= -40~85℃	100	—	—	Thousand times
tRET	Data retention period	TA = 105℃	20	—	—	years

(1) It is derived from comprehensive evaluation and is not tested in production.

4.1.18 Absolute maximum (electrical sensitivity)

Electrostatic Discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples, and the size of the sample is related to the number of power pins on the chip (3 x(n+1) power pins). This test meets the JEDECEIA /JESD22-A114 standard.

Table 26 Absolute maximum ESD values

symbol	argument	Condition	Maximum value (1)	unit
VESD(HBM)	Electrostatic discharge voltage (human model)	T A = +25 ° C, JEDEC compliant EIA/JESD22-A114	3000	V

(1) It is derived from comprehensive evaluation and is not tested in production.

4.1.19 Features of I/O ports

Common input/output features

Unless otherwise specified, the parameters listed in the following table are measured in accordance with general operating conditions. All I/O ports are compatible with CMOS and TTL.

Table 27I/O static characteristics

symbol	argument	Condition	Minimum value	Typical value	Maximum value	unit
VIL	Input low-level voltage	—		—	1.52	V

VIH	Standard I/O pin, input high level voltage		1.82	—	—	
	FT I/O pin, input high level voltage		1.82	—	—	
Vhys	Standard I/O pin Schmidt flip-flop voltage hysteresis	—	—	0.30	—	V
	5V tolerates I/O pin Schmidt trigger voltage hysteresis		—	0.30	—	V
Ilkg	Input leakage current	VSS ≤ VIN ≤ VDD Standard I/O port	—	—	±0.5	uA
		VIN = 5V, 5V tolerance port	—	—	±1	
RPU	Weak pull-up equivalent resistance	VIN = VSS	37	—	38.5	kΩ
RPD	Weak pull-down equivalent resistance	VIN = VDD	43.7	—	45.7	kΩ
CIO	Capacitance of the I/O pin			5		pF

Output voltage

Unless otherwise specified, the parameters listed in the following table are measured by ambient temperature and VDD supply voltage in accordance with common operating conditions. All I/O ports are compatible with CMOS and TTL.

Table 28 Output voltage characteristics

symbol	argument	Condition	Minimum value	Maximum value	unit
VOL	Output low	TTL port, I_{IO} = +12mA VDD=3.3V		0.4	V
VOH	Output high level		2.9		
VOL	Output low	CMOS port, I_{IO} = +14mA VDD=3.3V		0.4	
VOH	Output high level		2.9		
VOL	Output low	I_{IO} = +34mA VDD=3.3V		1.3	
VOH	Output high level		2		

4.1.20 NRST pin characteristics

The NRST pin input drive uses a CMOS process, which is connected to a pull-up resistor that cannot be disconnected.

Unless otherwise specified, the parameters listed in the following table are measured using ambient temperature and supply voltage conforming to common operating conditions.

Table 29NRST pin characteristics

symbol	argument	Condition	Minimum value	Typical value	Maximum value	unit
VIL(NRST)(1)	NRST Input low-level voltage	—	—	1.50	—	V
VIH(NRST)(1)	NRST input high level voltage	—	—	1.60	—	
Vhys(NRST)	NRST Schmidt flip-flop voltage hysteresis	—	—	100	—	mV
RPU	Weak pull-up equivalent resistance	VIN=VSS	—	41.5	—	kΩ
VF(NRST)(1)	NRST input filter pulse	—	—	120	—	ns
VNF(NRST)(1)	NRST input unfiltered pulse	—	25	—	—	ns

(1) Guaranteed by design, not tested in production.

Recommended NRST pin protection

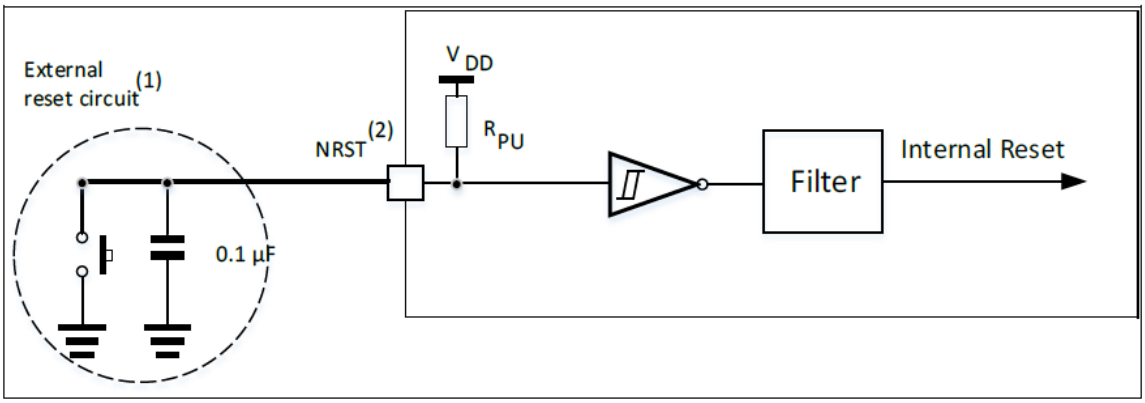


Figure 10 Suggested NRST pin protection

(1) The reset network is to prevent parasitic reset.
(2) The user must ensure that the potential of the NRST pin can be below the maximum VIL(NRST), otherwise the MCU cannot be reset.

4.1.21 TIM timer characteristics

The parameters listed in the following table are guaranteed by design.

Table 30TIMx features

symbol	argument	Minimum value	Maximum value	unit
tres(TIM)	Timer resolution time	1	—	tTIMxCLK
fEXT	External clock frequency of the timer CH1 to CH4	0	FTIMCLK/2	MHz
ResTIM	Timer resolution	—	16	位
tCOUNTER	16-bit counter clock cycle when internal clock is selected	1	65535	tTIMxCLK
tMAX_COUNT	Maximum possible count	—	65535*65535	tTIMxCLK

4.1.22 CAN(Controller Local Area Network) interface

For details about the features of the input/output multiplexing function pins (CAN_TX and CAN_RX), see the IO Port Features section.

4.1.23 12-bit ADC features

Unless otherwise specified, the parameters in the following table are measured using ambient temperature, fPCLK2 frequency and VDDA supply voltage in accordance with common operating conditions.

Note: It is recommended to perform a calibration each time you power on.

Table 31ADC characteristics

symbol	argument	Conditions	Minimum value	Typical value	Maximum value	unit
VDDA	Supply voltage	—	2.0	3.3	3.6	V
VREF+	Positive reference voltage	—	2.0	—	VDDA	V
fADC	ADC clock frequency	—	0.6	—	14	MHz

fS(2)	Sampling rate	—	0.05	—	1	MHz
fTRIG(2)	External trigger frequency	fADC = 14MHz	—	—	823	kHz
VAIN	Conversion voltage range (3)	—	0		VREF+	V
RAIN(2)	External input impedance	—	—	—	50	kΩ
RADC(2)	Sampling switch resistance	—	—	—	1	kΩ
CADC(2)	Internal sampling and holding capacitance	—	—	—		pF
tCAL(2)	Calibration time	fADC = 14MHz	5.9			us
			83			1/fADC
tlat(2)	Injection triggers the conversion delay	fADC = 14MHz	—	—	0.214	us
			—	—	3	1/fADC
tlatr(2)	Conventional trigger conversion time delay	fADC = 14MHz	—	—	0.143	us
			—	—	2	1/fADC
tS(2)	Sampling time	fADC = 14MHz	0.107	—	17.1	us
			1.5	—	239.5	1/fADC
tSTAB(2)	Power-on time	—	0	0	1	us
tCONV(2)	Total conversion time (including sampling time)	fADC = 14MHz			18	us
			14 to 252 (ts+ 12.5 for successive approximations)			1/fADC

(1) Guaranteed by comprehensive evaluation, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) Depending on the package, VREF+ can be internally connected to VDDA and VREF- can be internally connected to VSSA. See Chapter 3 for details.

(4) For external triggers, a delay 1/fPCLK2 must be added to the listed delay.

Table 32 Maximum RAIN when FADC =14 MHZ (1)

TS(period)	tS(us)	Maximum RAIN(kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	-
239.5	17.11	-

(1) Guaranteed by design, not tested in production.

4.1.24 DAC electrical parameters

Table 33DAC characteristics

symbol	argument	Minimum value	Typical value	Maximum value	unit	annotation
VDDA	Analog supply voltage	2.0	-	3.6	V	
VREF+	Reference voltage	2.0	-	3.6V	V	
VSSA	Ground wire	0	-	0	V	-
RLOAD(1)	Load resistance when the buffer is open	5	-	-	kΩ	-

RO(2)	Output impedance when the buffer is off	–	–	15	kΩ	–
CLOAD(1)	Load capacitance	–	–	50	pF	Large capacitance on DAC_OUT pin (when buffer is open)
DAC_OUT小(1)	The low end DAC_OUT voltage when the buffer is open	50	–	–	mV	The maximum DAC output span is given
DAC_OUT大(1)	High end DAC_OUT voltage when the buffer is open	–	–	VREF+ – 0.2	V	
DAC_OUT小(1)	The low end DAC_OUT voltage when the buffer is off	–	0.5	–	mV	The maximum DAC output span is given
DAC_OUT大(1)	High end DAC_OUT voltage when the buffer is off	–	–	VREF+ – 0.03	V	
DNL(2)	Nonlinear distortion (deviation between 2 consecutive codes -1LSB)	–	–	+–2	LSB	The DAC is configured with 12 bits
INL(2)	Nonlinear accumulation (deviation between the value measured at code i and the line between code DAC_OUT large and code DAC_OUT small)	–	–	+–4	LSB	The DAC is configured with 12 bits
Offset error (2)	Offset error (deviation between the value measured at code 0x800 and the ideal value V REF+ /2)	–	15	25	mV	When VREF+=3.3V, DAC Set this parameter to 12 bits
tSETTLING	Set time (full range: 10-bit input code changes from small value to large value, DAC_OUT reaches ±1 LSB of its final value)	–	3	4	us	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ
Update rate	When the input code is a small change (from the value i to i+1 LSB), the large frequency of the correct DAC_OUT is obtained	–	–	1	MS/s	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ
tWAKEUP	Wake time from off state (set ENx bit in DAC control register)	–	6.5	10	us	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ The input code is somewhere between a small and a large possible value
PSRR+ (1)	Supply rejection ratio (relative to V DDA)(static DC measurement)	–	-60	-50	dB	No R LOAD , C LOAD ≤ 50 pF

((1) Guaranteed by design, not tested in production.

(2) Guaranteed by comprehensive evaluation, not tested in production.

4.1.25 Temperature sensor characteristics

Table 34 Characteristics of temperature sensors

symbol	argument	Minimum value	Typical value	Maximum value	unit
Avg_Slope(1)	Average slope	—	4.3	—	mV/°C
V25(1)	Voltage at 25°C	—	1.18	—	V
tSTART(2)	Establishment time	—	—	10	us
TS_temp(2)(3)	ADC sampling time when reading temperature	—	—	17.1	us

(1) Guaranteed by comprehensive evaluation, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) The shortest sampling time can be determined by the application through multiple loops.

The temperature is obtained using the following formula:

The temperature(° C) = {(V25 - VSENSE) / Avg_Slope} + 25

Here (1) :

V25 = VSENSE value at 25 ° C

Avg_Slope = Temperature and the average slope of the VSENSE curve in mV/° C

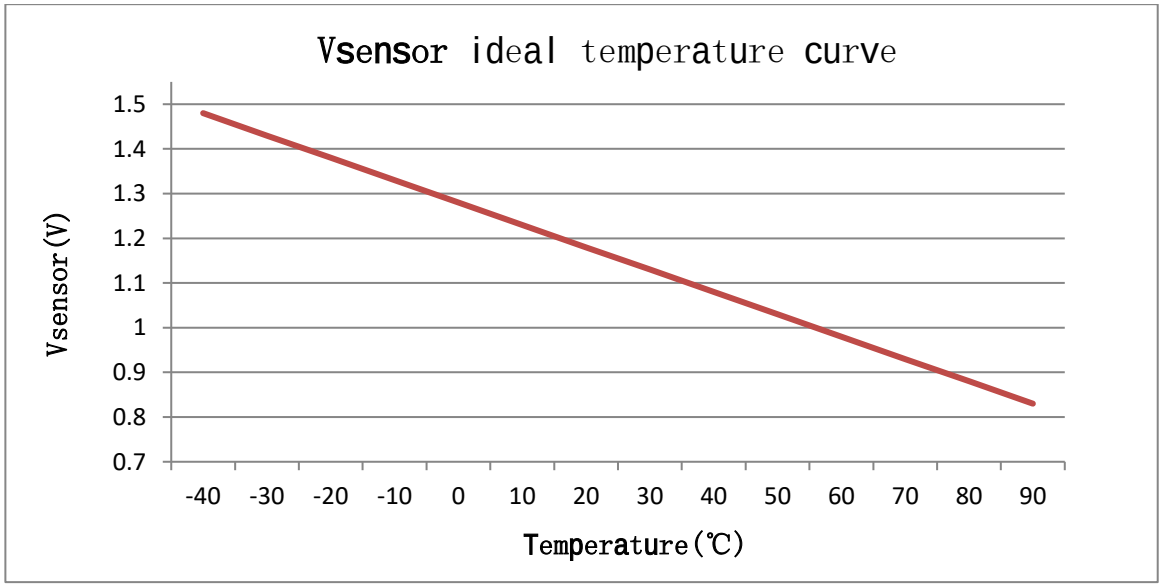
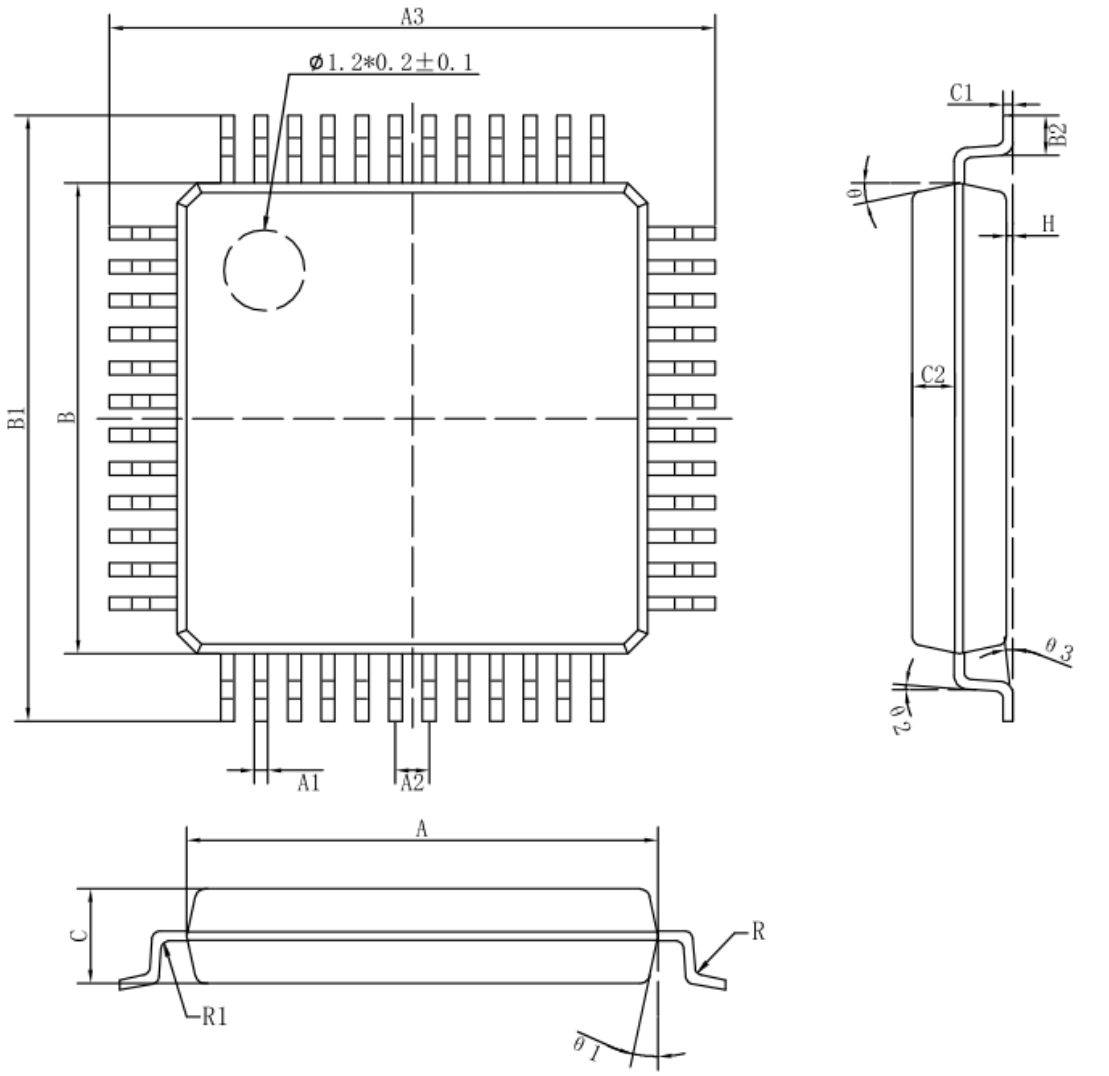


Figure 11V SENSE ideal curve for temperature

5 Package characteristics

LQFP48 package

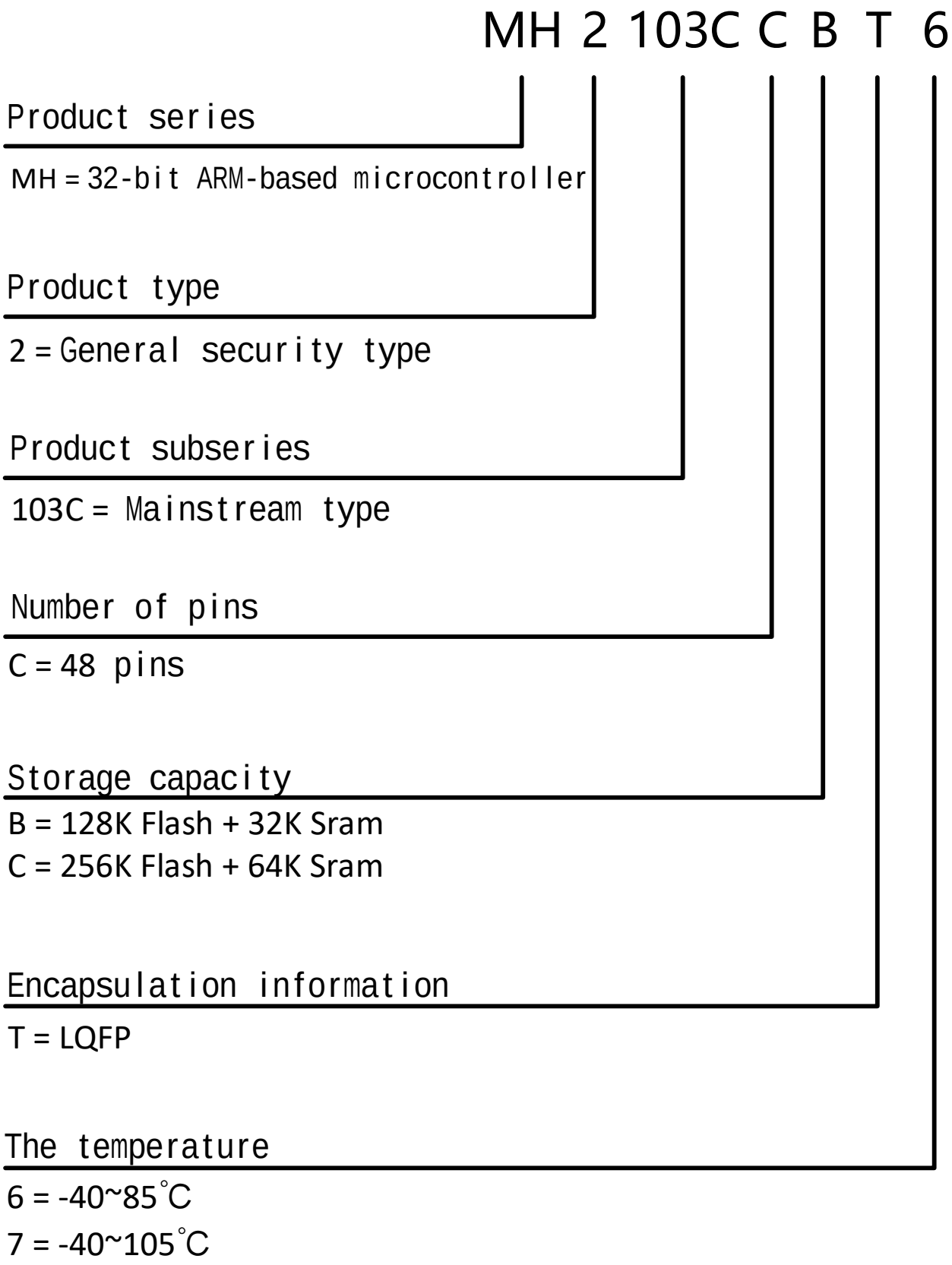


Dimension / Label	Minimum (mm)	Max (mm)	Dimension / Label	Minimum (mm)	Max (mm)
A	6.90	7.10	C2	0.636TYP	
A1	0.20TYP		H	0.05	0.15
A2	0.50TYP		θ	12° TYP4	
A3	8.80	9.20	θ1	12° TYP4	
B	6.90	7.10	θ2	4° TYP	
B1	8.80	9.20	θ3	0° ～ 5°	
B2	0.50	0.80	R	0.15TYP	
C	1.30	1.50	R1	0.12TYP	
C1	0.127	0.16			

Figure 12 LQFP487mm×7mm package size

6 Order code

Table 35 MH2103C series order code information diagram



7 Appendix

Table 36 Document version history

Date	Edition	Alter
2021-8-25	1.00	Initial version