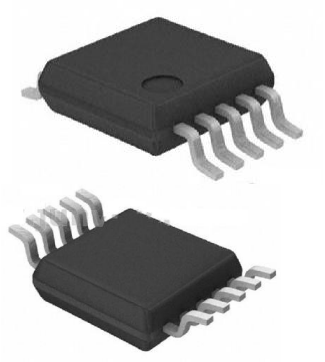
2.5V to 5.5V10Bit quad-channel digital-to-analog converter

Product description

The HS5314 is a 10bit four-channel output voltage DAC that is compatible with THS320, SPI, QSPI and Microwire serial ports. HS5314 data has 16 bits, including the DAC channel address, control bytes, and 10bitDAC data. The HS5314 power supply range is 2.5V to 5.5V.

HS5314 is packaged as HSOP10.



HSOP10

Main feature

- 10bit accuracy
- Established time 3us
- Low power consumption, 8mW at 5V and 3.6mW at 3V
- Integrate REF buffer
- Integrated output buffer
- Software Powerdown
- Supply voltage: 2.5V~5.5V

Apply

- Digital servo system control
- Digital compensation and gain adjustment
- Industrial process control
- Mechanical and mobile control equipment
- Mass storage device

Product specification classification

product	Encapsulation form	Screen name
HS5314	HSOP10	HS5314

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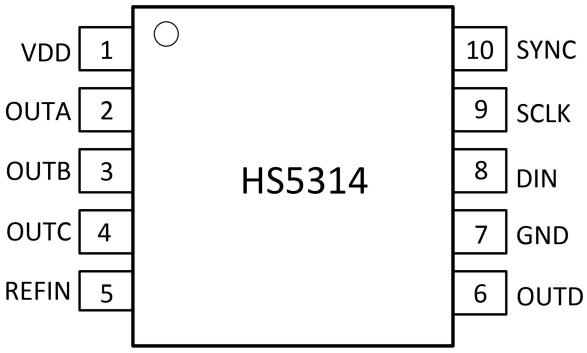
Pin plan



Pin specification

Pin number	Pin name	Pin attribute	Pin description
1	VDD	--	Power source
2	OUTA	O	Channel A analog output
3	OUTB	O	Channel B analog output
4	OUTC	O	Channel C analog output
5	REFIN	I	Reference input voltage
6	OUTD	O	Channel D analog output
7	GND	--	ground
8	DIN	I	Serial data entry
9	SCLK	I	Serial digital clock input
10	SYNC	I	Frame synchronization input signal

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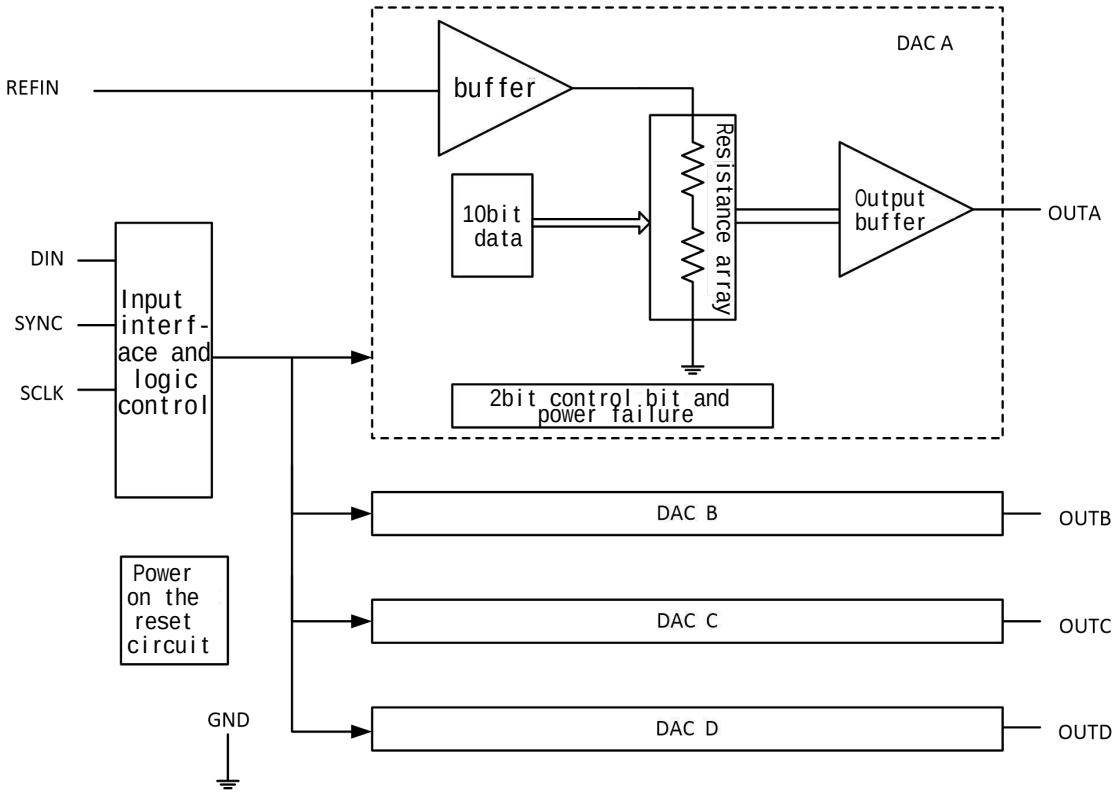
Internal block diagram



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Limiting parameter

Absolute maximum rating

Parameters	symbol	Parameter range	unit
Supply voltage	VDD	-0.3 ~ +7	V
Input digital voltage range	VIN	-0.3 ~ VDD+0.3	V
Reference input voltage range	VREFIN	-0.3 ~ VDD+0.3	V
Operating temperature range	TA	-40 ~ +105	°C
Storage temperature range	Tstg	-60 ~ +150	°C
Maximum junction temperature	Jt	150	°C
Welding temperature		260	°C

Recommended working conditions

Parameters		Minimum value	Typical value	Maximum value	unit
Supply voltage	5V power supply	4.5	5	5.5	V
	3V power supply	2.7	3	3.3	
Digital input high VIH	VDD=2.7V	2			V
	VDD=5.5V	2.4			
Digital input low level VIL	VDD=2.7V			0.6	V
	VDD=5.5V			1	
Reference voltage	(See Note 1)			VDD-1.5	V
Load resistance		2	10		KΩ
Load capacitance				100	pF
SCLK rate				20	MHz

Note 1: Input voltages greater than VDD/2 can result in output saturation at large DAC input codes.

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Electrical parameter

Static DAC parameters

Parameters		Test condition	Minimum value	Typical value	Maximum value	unit
precision				10		bits
Integral nonlinearity (INL)		See note 2		±0.5	±1	LSB
Differential nonlinearity (DNL)		See note 3		±0.5	±1	LSB
Zero offset		See note 4			±3	mV
Zero offset temperature drift		See note 5		-12		ppm/°C
Gain error		See note 6		±0.15	±3	%of FS Voltage
Gain error temperature drift		See note 7		12		ppm/°C
PSRR	zero	See note 8 and note 9		-80		dB
	Full width			-80		dB

Note: 2. Relative accuracy or integral nonlinearity (INL) refers to the linear error, which is the maximum deviation of the output from the ideal output excluding the zero error and the full amplitude error.
3. Differential nonlinearity (DNL), or differential error, refers to the largest variation adjacent to the LSB.
4. Analog output when the zero offset index word input is zero.
5. Zero offset Temperature drift index word input is zero when the analog output changes with temperature.
6. Gain error refers to the deviation between the analog output and the ideal output after removing the zero offset.
7. Gain error temperature drift refers to the change of the deviation of analog output and ideal output with temperature after removing the zero imbalance.
8. Zero power supply rejection ratio refers to when the digital input is all zero, VDD changes 5±0.5V and 3±0.3 lead to changes in the output.
9. Full amplitude output power rejection ratio refers to the change in output caused by VDD changes of 5±0.5V and 3±0.3V when the digital input is at full high power level.

DAC output parameter

Parameters	Test condition	Minimum value	Typical value	Maximum value	unit
Output voltage	RL=10kΩ	0		VDD-0.4	V
Output load adjustment accuracy	RL=2kΩ ~ 10kΩ		0.1	0.25	%of FS

Refer to input voltage parameters

Parameters	Test condition	Minimum value	Typical value	Maximum value	unit
Input voltage range	See note 10	0		VDD-1.5	V
Input resistance			10		MΩ
Reference feedthrough	REFIN=1Vpp(1KHz)+1.024 V （See note 11）		-75		dB
Reference input bandwidth	REFIN = 0.2Vpp+1.024V （Large signal）		1		MHz

Note: 10. Reference input voltage exceeding VDD/2 will result in output saturation distortion.

11. Reference Feedthrough refers to the analog output rejection ratio when the output digit is all zero and REFIN=1Vpp(1kHz)+1.024V.

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Digital input parameter

Parameters	Test condition	Minimum value	Typical value	Maximum value	unit
Digital input high level current	VI=VDD			±1	uA
Digital input low level current	VI=0V			±1	uA
Input capacitance			3		pF

Power consumption parameter

Parameters	Test condition	Minimum value	Typical value	Maximum value	unit
Supply current	5V power supply, no load, CLOCK, input 0V or VDD		1.6	2.4	mA
	3V power supply, no load, CLOCK, input 0V or VDD		1.2	1.6	mA
Drop-off current			10		nA

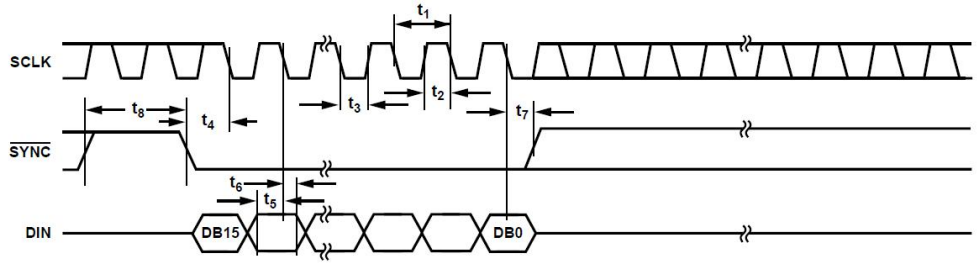
Simulation output dynamic parameters

Parameters	Test condition	Minimum value	Typical value	Maximum value	unit
SR	CL=100pF,RL=10kΩ,Vo＝10% to 90%，Vref=2.048,1.024		5		V/us
Ts	To ±0.5LSB，CL=100pF，RL=10kΩ		3	5.5	V/us
Ts(c)	To ±0.5LSB，CL=100pF，RL=10kΩ		1		us
Burr energy	From 1FF to 200		10		nV-sec
SNR	REFIN＝1.024 at 3V；REFIN=2.048 at 5V；fs=400kSPS，fout=1.1kHz sine wave，CL=100pF,RL=10kΩ,BW=20kHz		74		dB
S/(N+D)			66		
THD			-68		
SFDR			70		

Numerical input timing parameters

Parame-ters	Test conditions and annotations	Minimum and maximum time parameters		unit
		VDD=2.5V~3.6V	VDD=3.6V~5.5V	
t1	SCLK cycle	40	33	ns(min)
t2	SCLK High level time	16	13	ns(min)
t3	SCLK Low level time	16	13	ns(min)
t4	Establishment time of descending edge from SYNC to SCLK	16	13	ns(min)
t5	Data creation time	5	5	ns(min)
t6	Data retention time	4.5	4.5	ns(min)
t7	Time from SCLK falling edge to SYNC rising edge	0	0	ns(min)
t8	Minimum SYNC high level time	80	33	ns(min)

Sequence chart



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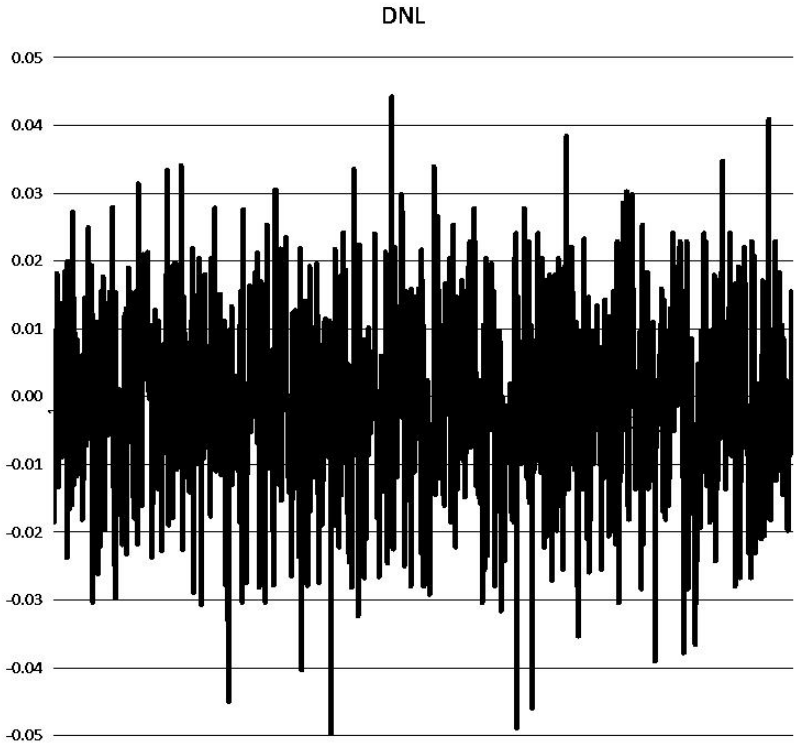
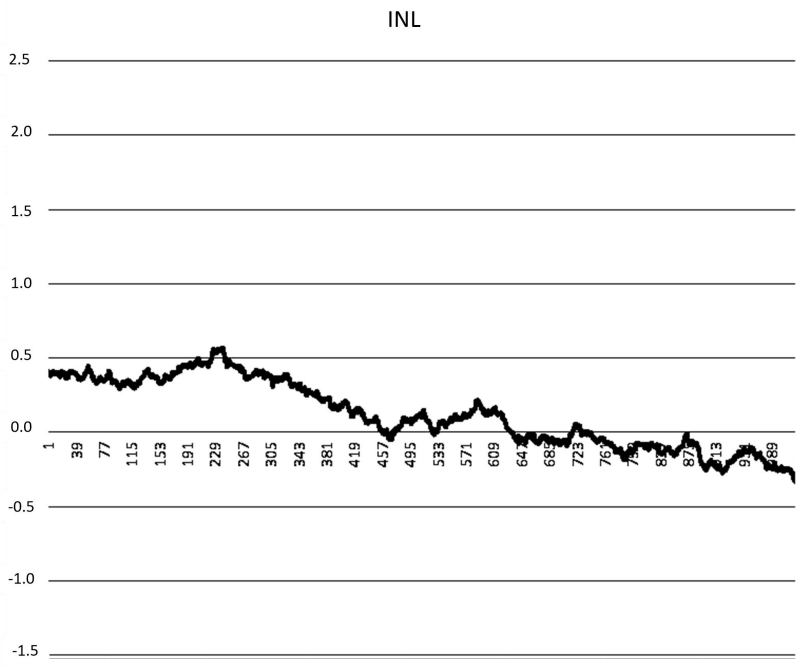
Typical graph





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Application description

Overall function

The HS5314 is a 10-bit single-supply digital-to-analog converter with a resistance array architecture that integrates serial interfaces, rate and turn-off logic controls, reference input buffers, resistance string, and output rail-to-rail buffers.

The output voltage can be expressed as:

$$Vout=\frac{VREF\times D}{2^N}$$

Where: D represents the decimal value of the code input to the digital-to-analog converter;

N indicates the accuracy of the converter;

Serial interface

The HS5314 digital input interface adopts the general 3-wire serial port mode, and the maximum operating frequency can reach 30MHz. It is compatible with standard SPI, QSPI, MICROWIRE and DSP interfaces.

The data word of HS5314 consists of two parts: the control bit (D15?D12) and the number bit (D9?D0). As shown in the picture below:

HSB LSB

A1	A0	PD	LDAC	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X
				←									→		

Data bit

A1 and A0 are the bits selected for the internal DAC channel address. The truth table is as follows:

A1	A0	DAC address
0	0	DAC-A
0	1	DAC-B
1	0	DAC-C
1	1	DAC-D

PD: 1 indicates the normal working mode; 0 indicates power failure mode, and the DAC output buffer indicates high resistance state.

LDAC: 1, update the data input register of the current address, but do not update the DAC register;

0, update to the output simultaneously according to the current four DAC registers;

Power supply bypass and ground management

In order to improve system performance, PCB design should be analog and digital respectively connected to different ground connection layers, the two floor surfaces should be connected together at the low impedance node of the system. It is best to connect the AGND of the DAC to the analog ground of the system to ensure that the analog ground current is well managed and that the voltage drop of the analog ground cable is negligible.

A 0.1uF ceramic decoupling capacitor should be connected between the chip power supply and the ground and installed as close to the chip as possible. The use of magnetic loops further separates the analog and digital power supplies of the system.

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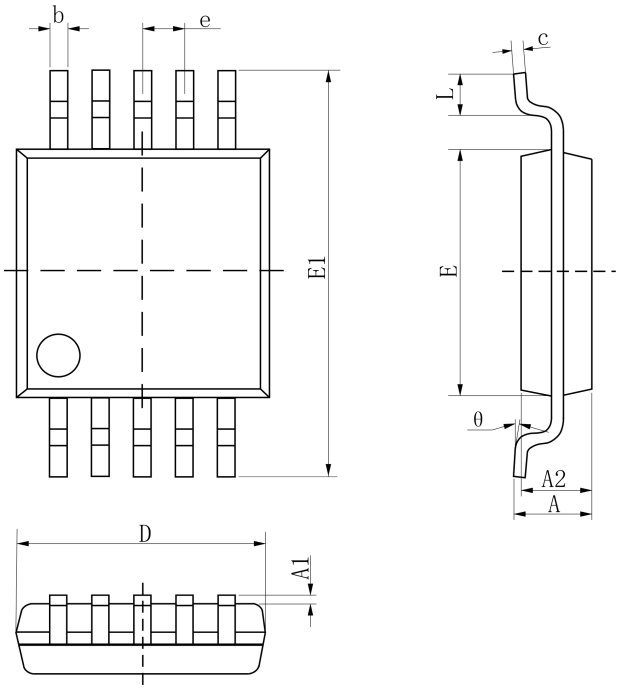
Package outline drawing

HSOP10



symbol	Size (mm)		Size (inches)	
	minimum	Max	minimum	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.50BSC		0.020BSC	
L	0.400	0.800	0.016	0.031
θ	0º	6º	0º	6º

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Seal and packing specification

1. Seal content introduction

Product model：HS5314

Production lot number：XXXXXXX

2. Seal specification

Laser print, centered and Arial font.

3. Packing specification

Model number	Encapsulation form	Pieces/ roll	Reel/box	Pieces/box	Box/box	Pieces/box
HS5314	HSOP10	3000	1	3000	8	24000

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Statement

- Hongli Kunpeng reserves the right to change the instructions without prior notice! Customers should obtain the latest version of the information and verify that the relevant information is complete before placing an order.
- When using Hongli Kunpeng products for system design and complete machine manufacturing, the buyer has the responsibility to comply with safety standards and take appropriate safety measures to avoid personal injury or property damage caused by potential failure risks!
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MOS circuit operation precautions

Static electricity will be generated in many places, take the following preventive measures, can effectively prevent the MOS circuit due to the impact of electrostatic discharge caused by damage:

1. The operator should ground the ground using an ESD wrist strap.

2, the equipment shell must be grounded.

3, the tools used in the assembly process must be grounded.

4, must use conductor packaging or antistatic materials packaging or transportation.

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