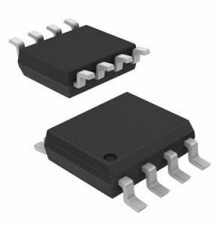
2.7V to 5.5V, serial input, voltage output, 16-bit digital-to-analog converter

Product description

The HS5541/HS5542 is a single-channel, 16-bit, serial input, voltage output DTO converter powered by a single supply from 2.7V to 5.5V with an output range of 0V to VREF . Monotonicity is guaranteed across the output range, providing 14-bit accuracy of 1LSB INL at temperatures ranging from -40 ° C to +85 ° C. The HS5541/HS5542 offers unbuffered output, low setup time, low power consumption and low offset errors. And has low noise performance and low burr, suitable for a variety of terminal systems.

The HS5542 is capable of operating in bipolar mode, producing ±VREF output swing. Features Kelvin detection connections for reference voltage and analog ground pins to reduce layout sensitivity.



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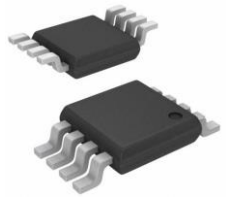

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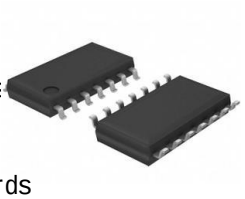

SOP14

MSOP10

Main feature

- Effective accuracy 14 bits
- 3V and 5V single power supply
- Low power consumption: 0.825mW
- Establishment time:1.2μs
- The unbuffered voltage output can directly drive 60kΩ loads
- Low burr: 1.1nV-s
- Compatible with SPI/QSPI/MICROWIRE and DSP interface standards

Apply

- Precision source measuring instrument
- Automatic test equipment
- Data acquisition system
- Process control

Product specification classification

product	Encapsulation form	Screen name
HS5541	SOP8	HS5541
*HS5541M	MSOP8	HS5541M
HS5542	SOP14	HS5542
*HS5541A	MSOP10	HS5541A

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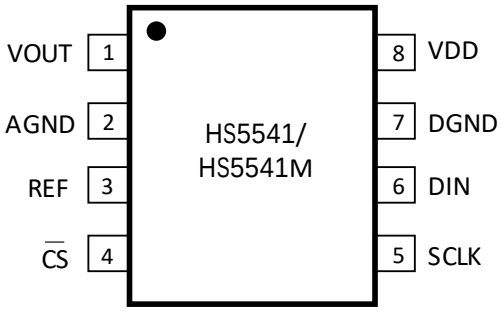
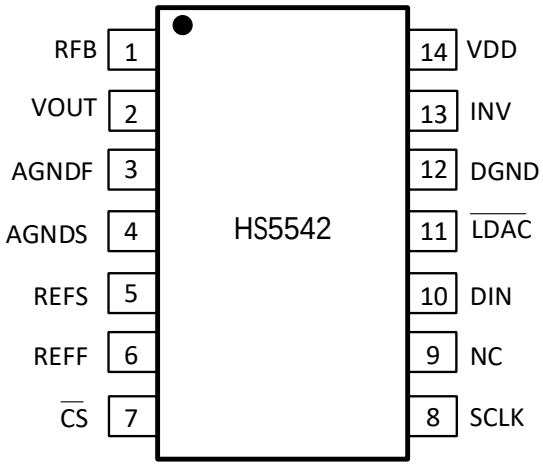
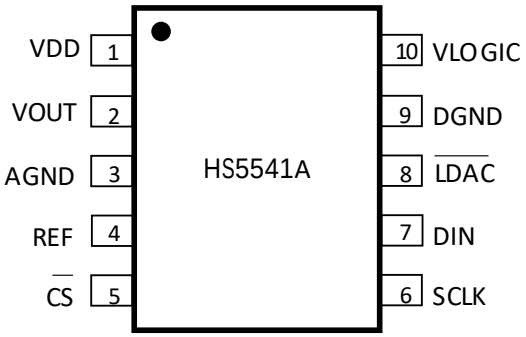
Pin plan







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Pin specification

Pin number	Pin name	Pin attribute	Pin description
HS5541/HS5541M			
1	VOUT	O	Analog output voltage of DAC
2	AGND	-	Analog reference site
3	REF	I	The DAC refers to the input voltage and connects the external 2.5V, voltage range 2V to V_{DD}
4	CS	I	Logic input signal, chip signal selection side for serial data input control
5	SCLK	I	Clock input, rising edge triggers data into the register
6	DIN	I	Serial data input, which can support 16 bits of data, enters the register when SCLK rises the edge
7	DGND	-	Digital reference site
8	VDD	-	Power source
HS5542			
1	RFB	O	Resistive feedback pins, in bipolar mode, connect the external op-amp output
2	VOUT	O	Analog output voltage of DAC
3	AGNDF	-	Analog reference site
4	AGNDS	-	Analog reference site
5	REFS	I	The DAC refers to the input voltage (detection) to connect the external 2.5V, voltage range 2V to V_{DD}
6	REFF	I	The DAC refers to the input voltage (load) to connect the external 2.5V, voltage range 2V to V_{DD}
7	CS	I	Logic input signal, chip signal selection side for serial data input control
8	SCLK	I	Clock input, rising edge triggers data into the register
9	NC	-	unconnected
10	DIN	I	Serial data input, can support 16 bits, data into the register when SCLK rising edge
11	LDAC	I	When the input low power level, the DAC register and serial register data content are updated synchronously
12	DGND	-	Digital reference site
13	INV	O	Connect to the scaling resistor inside the DAC, and connect to the inverting input of the external op amp in bipolar mode
14	VDD	-	Power source

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Pin number	Pin name	Pin attribute	Pin description
HS5541**A**			
1	VDD	-	Power source
2	VOUT	O	Analog output voltage of DAC
3	AGND	-	Analog reference site
4	REF	I	The DAC refers to the input voltage and connects the external 2.5V, voltage range 2V to V_{DD}
5	CS	I	Logic input signal, chip signal selection side for serial data input control
6	SCLK	I	Clock input, rising edge triggers data into the register
7	DIN	I	Serial data input, which can support 16 bits of data, enters the register when SCLK rises the edge
8	LDAC	I	When the input low power level, the DAC register and serial register data content are updated synchronously
9	DGND	-	Digital reference site
10	VLOGIC	-	Logic power supply

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Internal block diagram

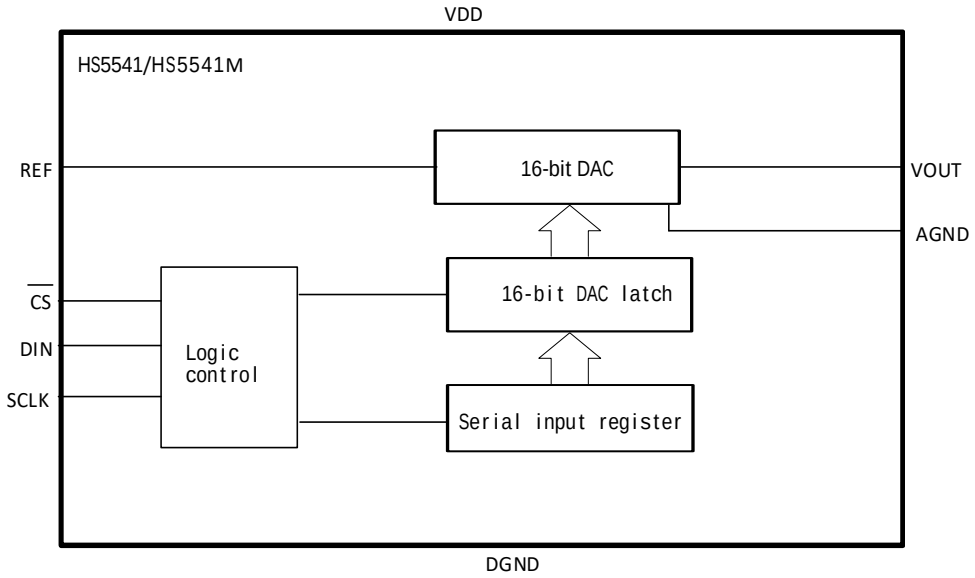

Figure 1. HS5541/HS5541M structure diagram

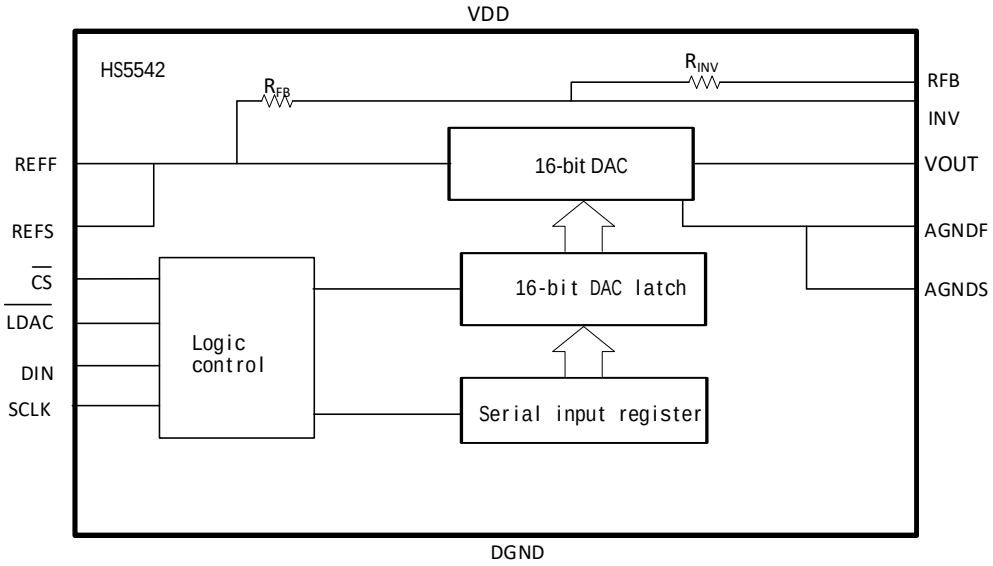

Figure 2. HS5542 structure diagram

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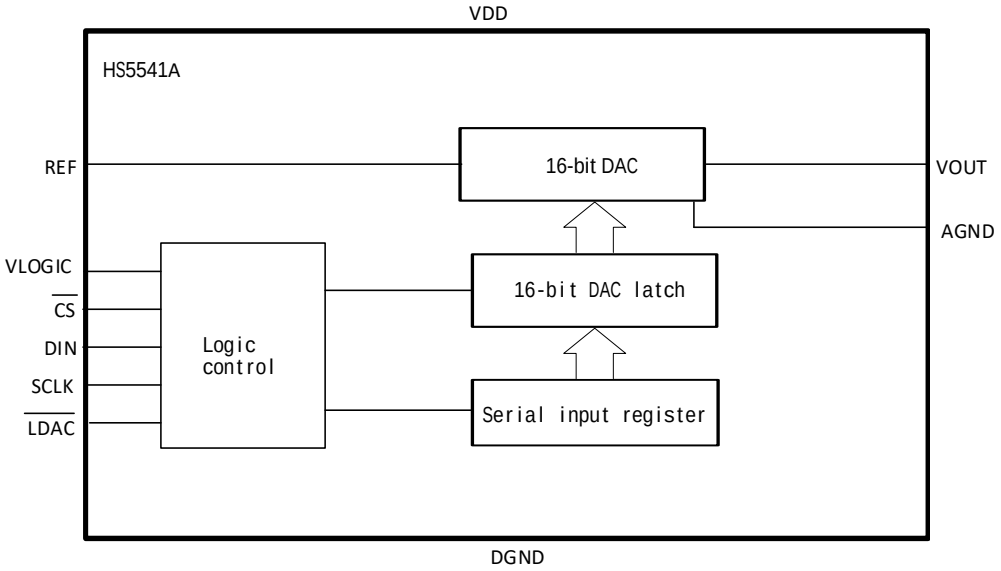

Figure 3. HS5541A structure diagram

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Limiting parameter

In the use of the chip, any application mode that exceeds the limit parameter will cause permanent damage to the device, and the reliability of the chip may be affected if the chip is in the limit working state for a long time. The limit parameters are only derived from a series of extreme tests, and do not mean that the chip can work normally under this limit condition. DGND=AGND=0V, all voltage values are relative to 0V.

argument	symbol	Rated value	unit
Supply voltage	V_{DD}	-0.3 ~ +6.0	V
Input current	I_{in}	±10	mA
Operating ambient temperature[1]	T_A	-40 ~ +85	°C
Storage temperature[1]	T_{stg}	-65 ~ +150	°C
ESD	HBM	>±3k	V

Note 1: Except for the items of operating ambient temperature and storage temperature, all temperatures are T_A = 25°C。

Recommended working conditions

Operating power supply voltage range

argument	symbol	Parameter range			unit
		minimum	Standard	Max	
Supply voltage range	V_{DD}	2.7	5	5.5	V
Reference voltage range	V_{REF}	2	2.5	V_{DD}	V

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Electrical parameter

V_{DD}=2.7V ~ 5.5V，V_{REF}=2V ~ V_{DD}，AGND=DGND=0V，T_A=T_{MIN} ~ T_{MAX} 。

Note: There is no special requirement that the ambient temperature is T_A= 25°C ±2°C。

argument	Test condition	Minimum value	Typical value	Maximum value	unit
Static characteristic					
Resolution		14			bits
Integral nonlinearity	V_{REF}=2.048V，V_{DD}=5V，T_A=25℃		±6.5	±10.5	LSB
Differential nonlinearity			±4	±5	LSB
Gain error	T_A=25℃		±2	±5	LSB
Gain error temperature coefficient			±0.1		ppm/°C
Unipolar zero code error	T_A=25℃		±2	±2.5	LSB
Unipolar zero code error temperature coefficient			±0.05		ppm/°C
HS5542					
Bipolar zero offset error	T_A=25℃		±2	±5	LSB
Bipolar zero temperature coefficient			±0.2		ppm/°C
Bipolar zero code offset error	T_A=25℃		±2	±5	LSB
Bipolar gain error	T_A=25℃		±2	±5	LSB
Temperature coefficient of bipolar gain			±0.1		ppm/°C
Output characteristic					
Output voltage range	Unipolar mode	0		V_{REF}-1LSB	V
	HS5542 bipolar mode	- V_{REF}		V_{REF}-1LSB	μs
Output voltage setup time	C_L=10pF		1.2		μs
Conversion rate	C_L=10pF，0%-63%		4		V/us
Digital to analog burr pulses	1LSB		18		nV-sec
Digital feedthrough	V_{REF}=2.048V		0.2		$nV/\sqrt{Hz}$
Output noise density	DAC code=0×8400,f=1kHz		11.8		μVp-p
Output noise voltage	f=0.1Hz ~10Hz		0.134		LSB
Power supply rejection ratio	ΔV_{DD}±10%			±1.0	V
DAC reference input					
Reference input range		2.0		V_{DD}	V
Reference input impedance[2]	Unipolar mode	13.5			kΩ
	HS5542 bipolar mode	11.5			kΩ

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argument	Test condition	Minimum value	Typical value	Maximum value	unit
Logical input					
Input current				±1	μA
Input undervoltage				0.8	V
Input high voltage		2.4			V
Input capacitance				10	pF
Lag voltage			0.15		V
Supply voltage					
Supply voltage		2.7		5.5	V
current	The number input is 0		165	227	μA
Power dissipation	The number input is 0		0.825	1.248	mW

Note 2: Reference input resistance is code dependent. When Code=0x8555, the reference input impedance is minimum.

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Clock characteristic

Where not specified: V_{DD}=2.7V ~ 5.5V±10%, V_{REF}=2.048V, V_{INH}= 90% of V_{DD}, V_{INL}= 10% of V_{DD}, AGND=DGND=0V, -40℃< T_A <+85℃。

argument	Description	Numerical value	unit
f_{SCLK}	SCLK cycle frequency	20	MHz
t1	SCLK cycle time	50	ns min
t2	SCLK High level time	25	ns min
t3	SCLK Low level time	25	ns min
t4	The establishment time from low CS to high SCLK	30	ns min
t5	The establishment time from high CS to high SCLK	45	ns min
t6	SCLK high to CS low retention time	45	ns min
t7	SCLK high to CS high retention time	30	ns min
t8	Data start time	20	ns min
t9	Data retention time	10	ns min
t10	LDAC Pulse width	60	ns min
t11	CS high to LDAC low	60	ns min
t12	CS is the high effective time	60	ns min

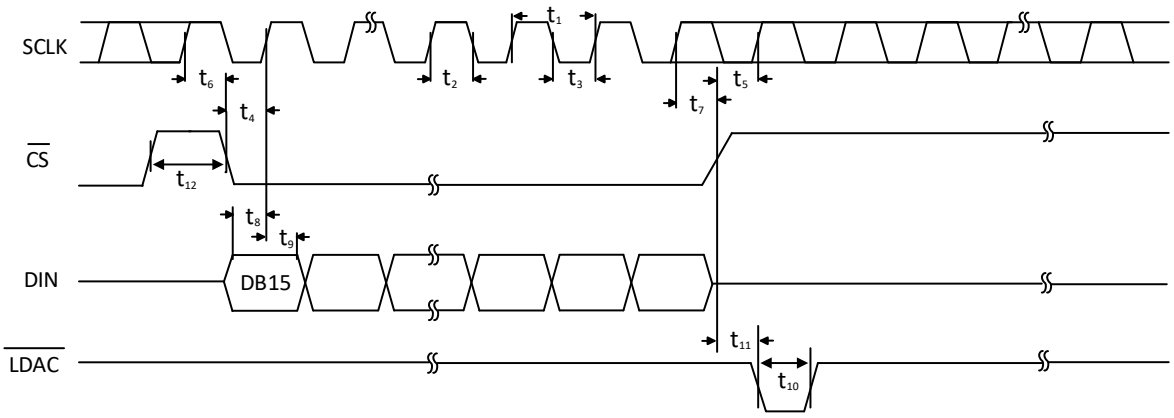

Figure 4. Timing diagram

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Typical characteristic curve

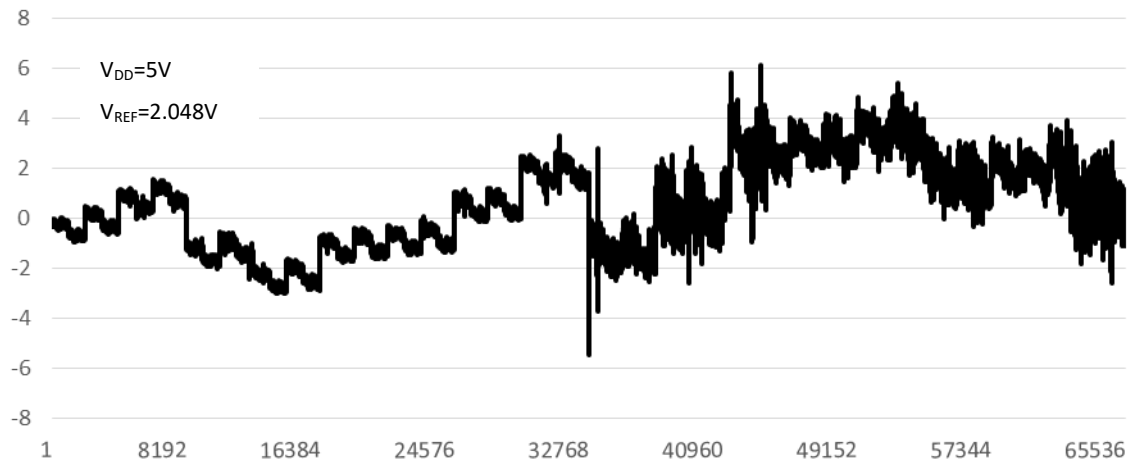

Figure 5. Integral nonlinearity VS. codes

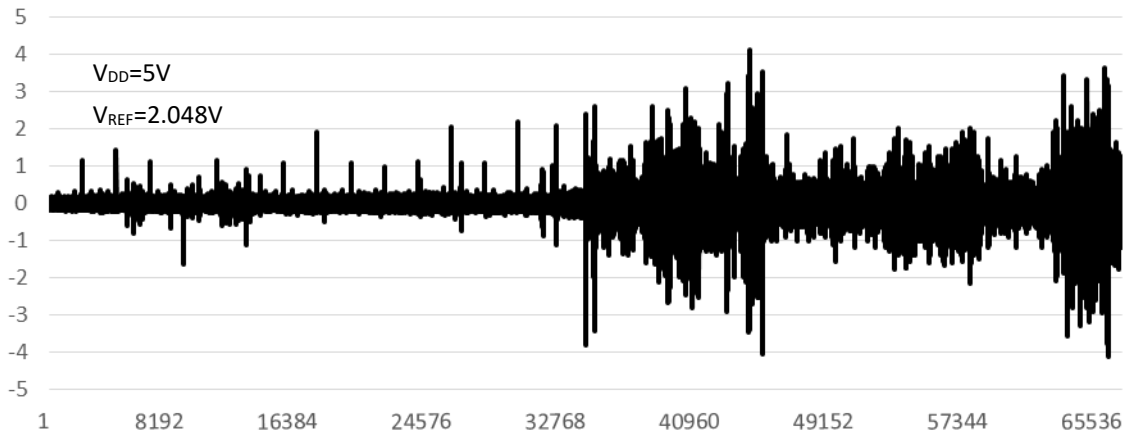

Figure 6. Differential nonlinearity VS. code

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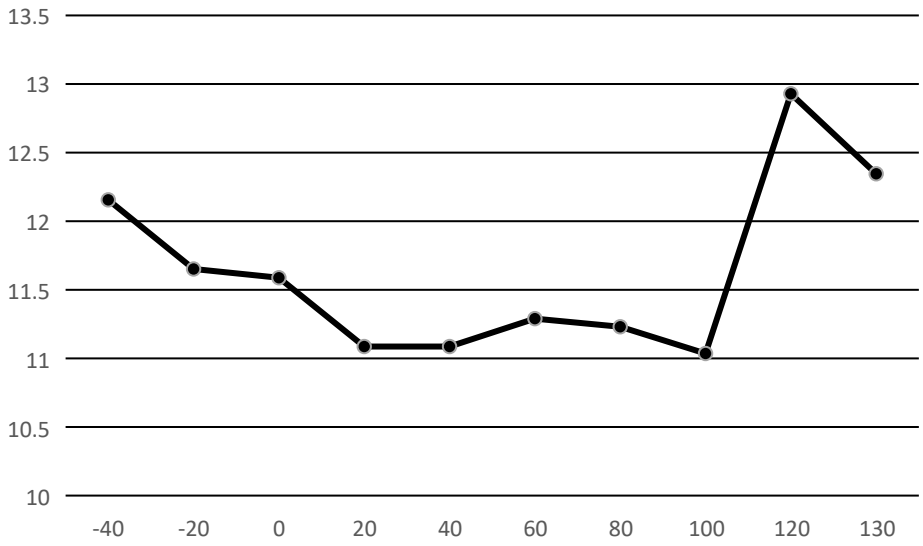

Figure 7. HS5542- Integral nonlinearity VS. temperature

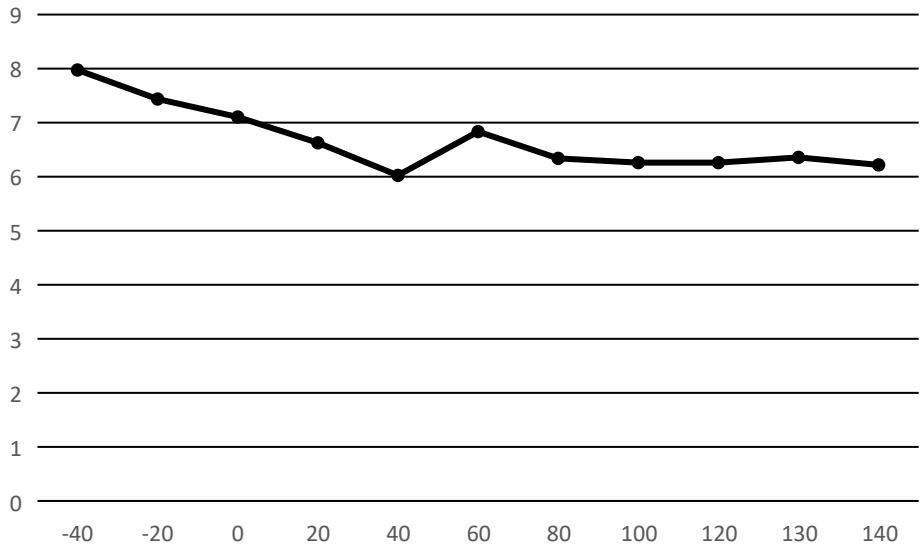

Figure 8. HS5542- Differential nonlinearity VS. temperature

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Working principle

The HS5541/HS5542 is a single-channel, 16-bit, serial input, voltage output DAC. The operating voltage range is 2.7V to 5.5V, and the typical power consumption with a 5V supply is 165μA. Data is written to the device in 16-bit word format via a three - or four-wire serial interface. To ensure a known power-on state, the device is designed with a power-on reset function. HS5541 in unipolar mode has an output of 0V, and HS5542 in bipolar mode has an output of -V_{REF}. The HS5542 has a reference voltage and analog ground for Kelvin detection connections.

Digital to analog conversion part

The DAC architecture consists of two matching DAC sections. FIG. 7 shows a simplified circuit diagram. The HS5541/HS5542 uses a segmented DAC architecture. After decoding the high 4 bits of the 16-bit data, 15 switches from E1 to E15 can be driven. Each switch connects one of 15 matching resistors to either AGND or V_{REF}. The remaining 12 bits in the 16-bit data drive the voltage mode R-2R ladder network's S0 to S11 switches.

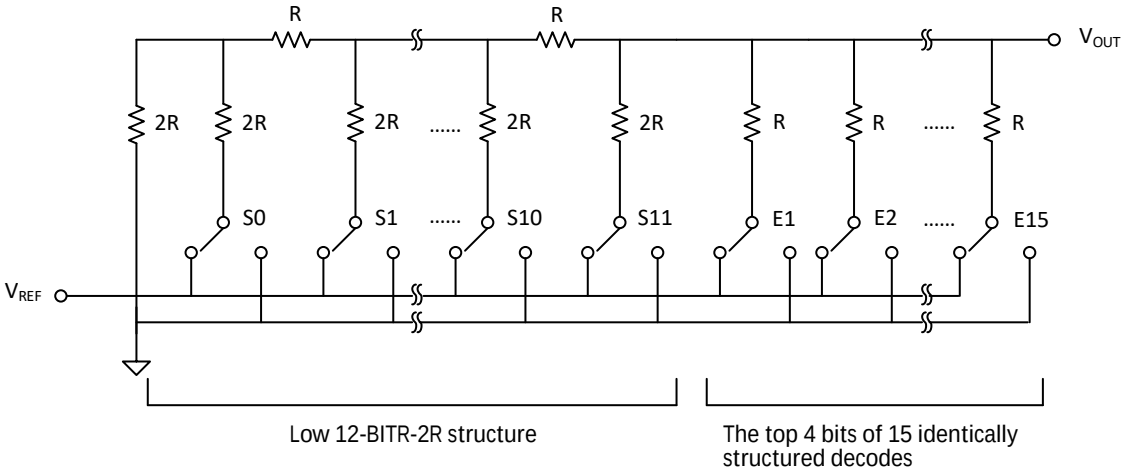

Figure 7. DAC structure

With this DAC configuration, the output impedance is code independent, while the input impedance of the reference voltage source is highly code dependent. The output voltage is related to the reference voltage, as shown below:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

Where: D is the decimal data word loaded into the DAC register. N is the resolution of the DAC. For 2.5V reference voltage, the above formula can be simplified to the following formula:

$$V_{OUT} = \frac{2.5 \times D}{65536}$$

Thus, the DAC loads the intermediate level code with a VOUT of 1.25V and loads the full scale code with a VOUT of 2.5V. The LSB size is V_{REF} /65536.

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Serial interface

The HS5541/HS5542 is controlled by a multifunctional three - or four-wire serial interface, capable of operating at clock rates up to 20MHz and compatible with SPI, QSPI, MICROWIRE and DSP interface standards. The timing diagram is shown in Figure 4. In addition to the 16-bit DAC register, HS5541/HS5542 has a separate serial input register into which new data values can be preloaded without interfering with the existing DAC output voltage.

Input data by slice select input $\overline{CS}$ enables frame transfer. After a high-low jump on the $\overline{CS}$, data is synchronously moved in on the rising edge of the serial clock SCLK and locked in the serial input register. After all 16 data bits are loaded into the serial input register, a low-high transition occurs on the $\overline{CS}$, and if the $\overline{LDAC}$ is low, the contents of the shift register are transferred to the DAC register. If the $\overline{LDAC}$ is at a high level at this time, the low high jump on the $\overline{CS}$ will only transfer that content to the serial input register. After the new value is fully loaded into the serial input register, it can be asynchronously transferred to the DAC register via a gating pin. Data is loaded as a 16-bit word, with MSB taking precedence. Only $\overline{CS}$ at low power level can load data into the device.

Unipolar output structure

The DAC is capable of driving 60K unbuffered loads. Unbuffered operation results in low supply current (typical 300μA) and low offset errors. The unipolar output swing of the HS5541 is 0V to V_{REF}. Figure 8 shows a typical unipolar output voltage circuit. This example uses a 2.5V reference and a low offset, zero drift reference voltage buffer HS8629.

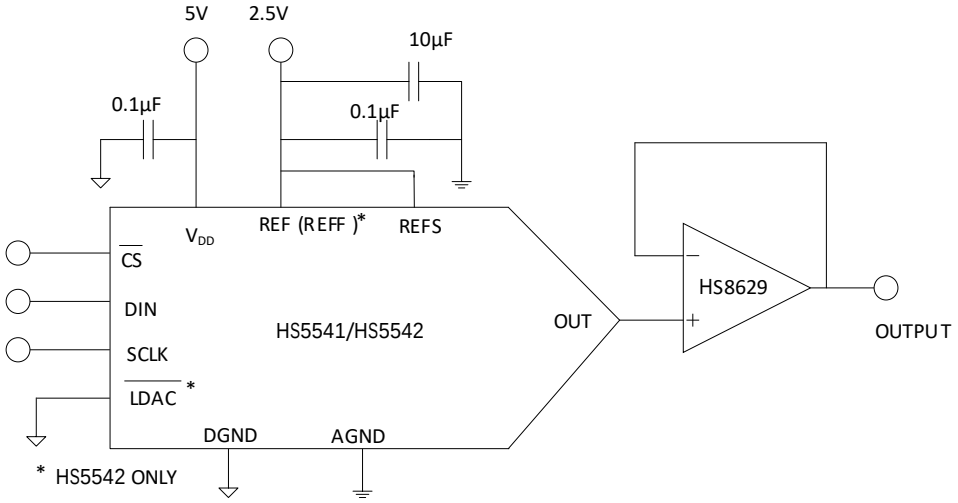

Figure 8. Unipolar output circuit structure

Assuming an ideal reference voltage source is used, the unipolar worst-case output voltage can be calculated by:

$$V_{OUT-UNI}=\frac{D}{2^{16}}\times\left(V_{REF}+V_{GE}\right)+V_{ZSE}+INL$$

$V_{OUT-UNI}$ indicates the worst-case output of unipolar mode. D is the code that loads the DAC . V_{REF} is the reference voltage applied to the device. V_{GE} is the gain error in volts (V). V_{ZSE} is zero level error in volts (V). INL is integral nonlinear in volts (V).

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Bipolar output structure

The HS5542 is capable of providing a bipolar output for the peripherally connected op amp, and a typical circuit structure is shown in Figure 9 below. Among them, R_{INV} and R_{FB} with a typical value of 28kΩ are connected to the input and output of the op amp as feedback resistors to achieve bipolar output.

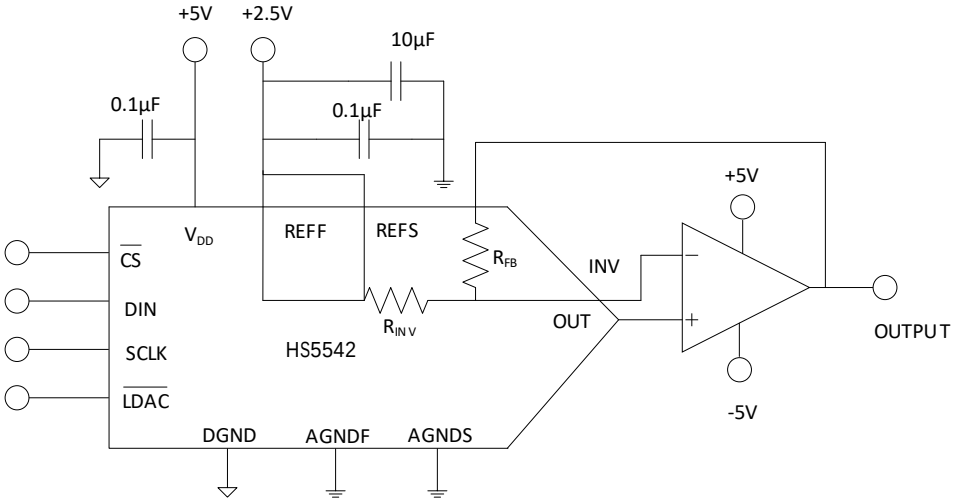

Figure 9. Bipolar output circuit structure

Assuming an ideal reference voltage source is used, the bipolar worst-case output voltage can be calculated by the following formula:

$$V_{OUT-BIP}=\frac{\left[\left(V_{OUT-UNI}+V_{OS}\right)\left(2+RD\right)-V_{REF}\left(1+RD\right)\right]}{1+\left(2+RD\right)/A}$$

$V_{OUT-BIP}$ is the worst-case output of bipolar mode. $V_{OUT-UNI}$ is the worst case output in unipolar mode. V_{OS} is the input offset voltage of the external op amp. RD is the matching error between R_{FB} and R_{INV} resistance. A is the open-loop gain of the op amp.

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Typical application

Layout guide

In any circuit where precision is important, careful consideration of the layout of the power supply and ground loop helps ensure that the specified performance is achieved. The printed circuit board (PCB) used in the installation of HS5541/HS5542 shall be designed with the analog part separate from the digital part and confined to a certain area of the board. If the HS5541/HS5542 system has multiple components requiring analog-digital connection, the connection can only be made at one point. The star ground point is as close to the device as possible. The HS5541/HS5542 should have a sufficiently large 10μF power supply bypass capacitor in parallel with the 0.1μF capacitor on each power supply and as close to the package as possible, preferably directly against the device. The 10μF capacitor is a tantalum bead capacitor. The 0.1μF capacitor should have a low effective series resistance (ESR) and a low effective series inductance (ESI), such as a common ceramic capacitor that provides a low impedance ground path at high frequencies, in order to handle the transient current caused by the internal logic switch.

Optical coupler circuit

HS5541/HS5542 are Schmidt triggered digital inputs that allow them to receive slow digital transmissions. These are suitable for industrial applications where it may be necessary to isolate the DAC from the controller via an optocoupler, the optocoupler isolation circuit structure shown in Figure 10 below.

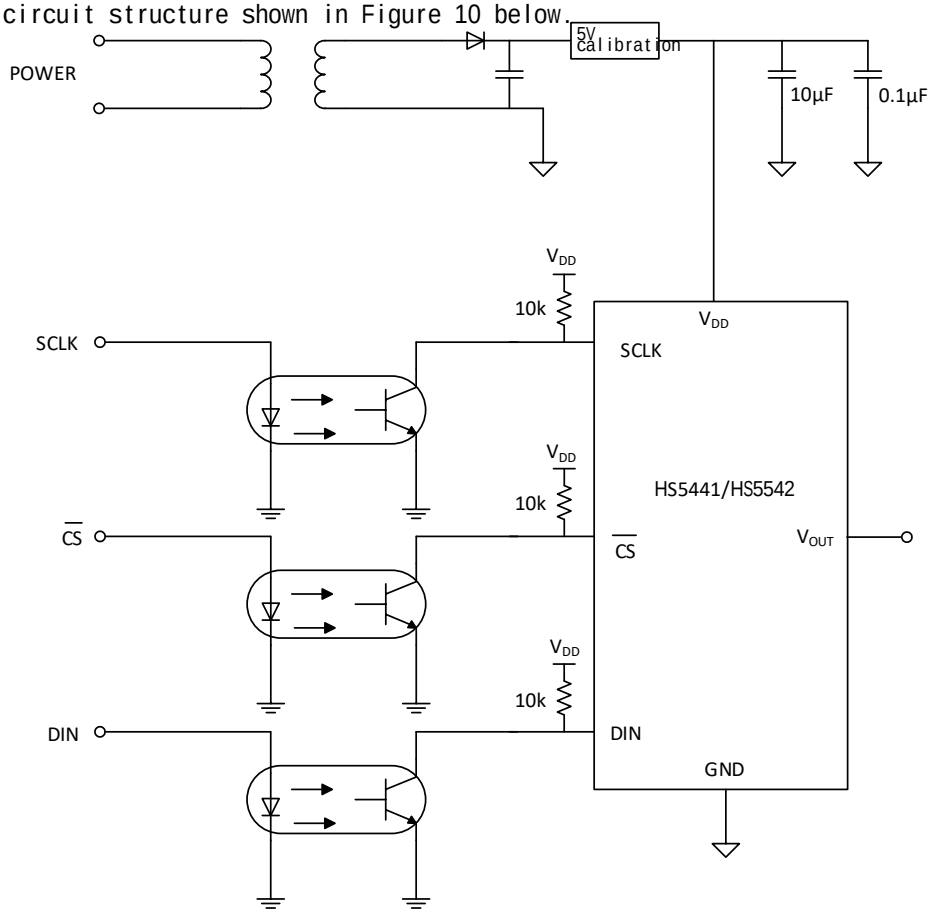

Figure 10. Optical coupler interface circuit block diagram

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Multichannel decoding circuit

The HS5541/HS5542 has a chip selector pin $\overline{CS}$ that allows one or more Dacs to be selected to work together. All chips receive the same clock string and data string, but only one chip can receive the $\overline{CS}$ signal at a time. The address of the DAC is determined by the decoder. There is a phenomenon of digital feed-through on the digital channel, and the effect of digital feed-through on the analog signal channel can be minimized by using the burst clock. The typical circuit structure is shown in Figure 11.

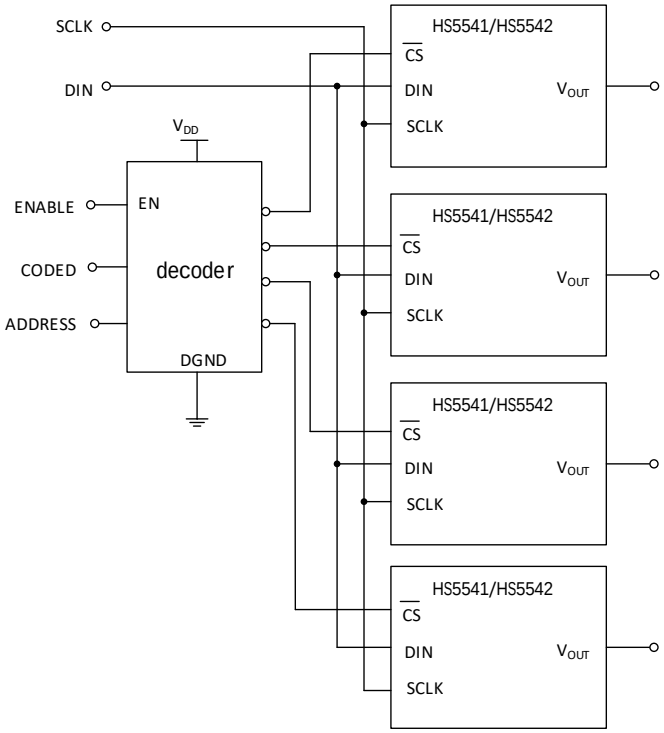

Figure 11. Multiplex DAC

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Package outline drawing

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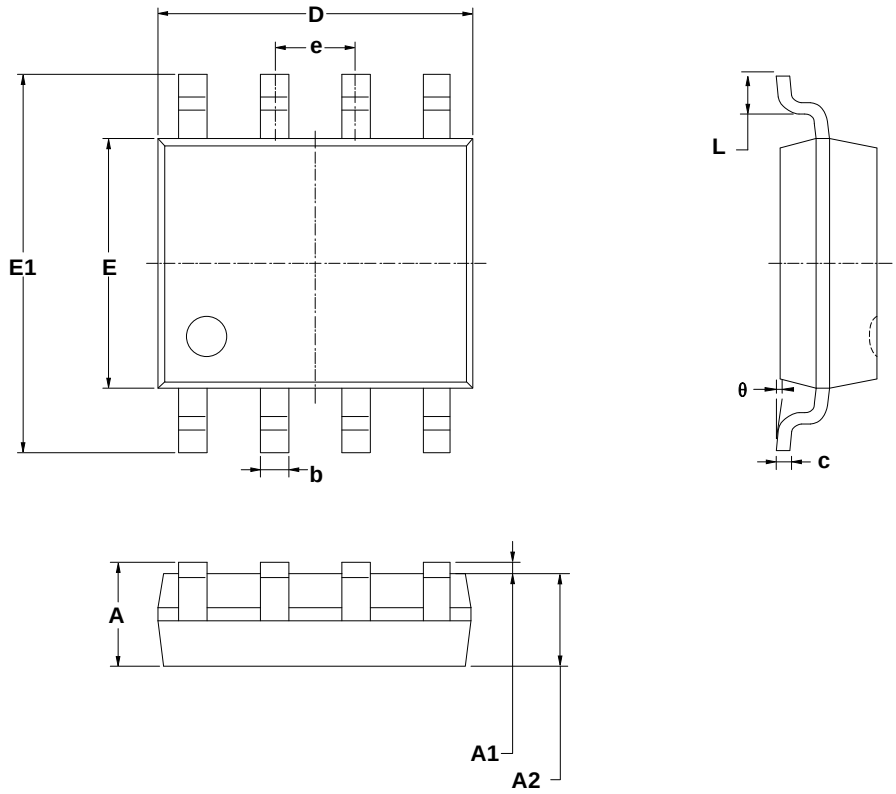

symbol	Size (mm)		
	minimum	model	Max
A			1.75
A1	0.10		0.225
A2	1.30	1.40	1.50
b	0.39		0.47
c	0.20		0.24
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27BSC		
L	0.50		0.80
θ	0°		8°

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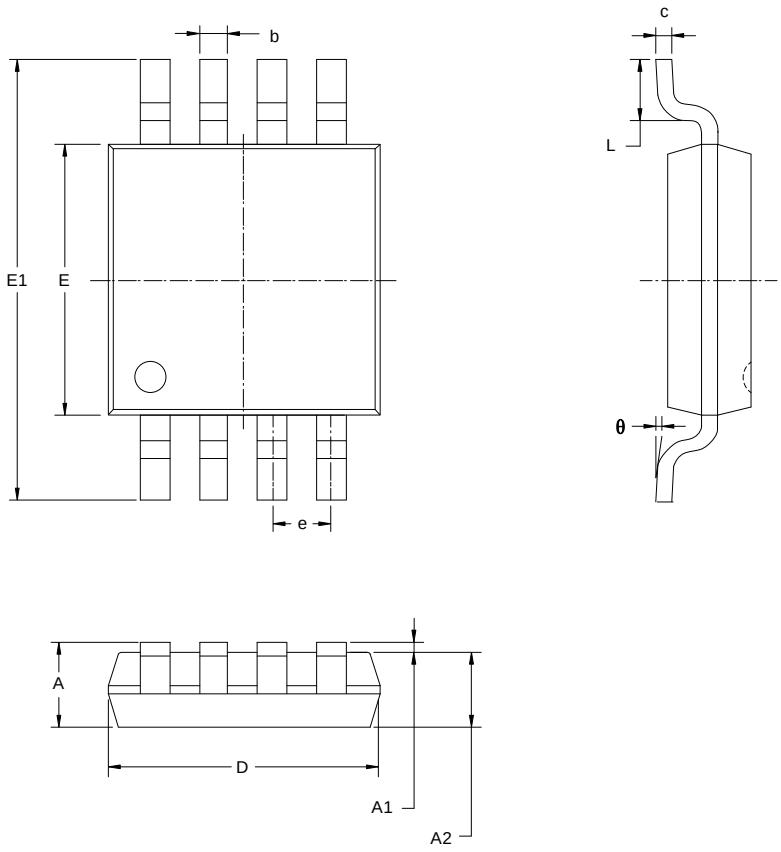
MSOP8



symbol	Size (mm)		
	minimum	model	Max
A			1.10
A1	0.05		0.15
A2	0.75	0.85	0.95
b	0.28		0.36
c	0.15		0.19
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.70	4.90	5.10
e	0.65BSC		
L	0.40		0.70
θ	0°		8°

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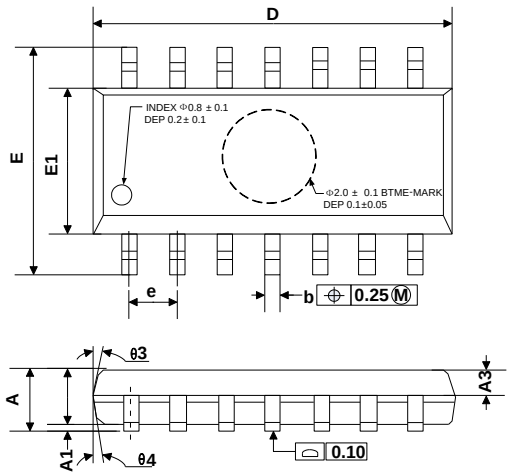
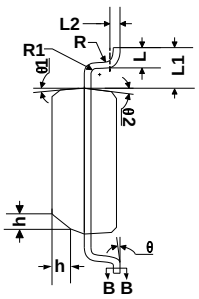
SOP14





symbol	Size (mm)		
	minimum	model	Max
A	1.35		1.75
A1	0.10		0.25
A2	1.25		1.65
A3	0.55		0.75
D	8.53		8.73
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
L	0.45		0.80
L1	1.04 REF		
L2	0.25 BSC		
R	0.07		
R1	0.07		
h	0.30		0.50
θ	0°		8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°

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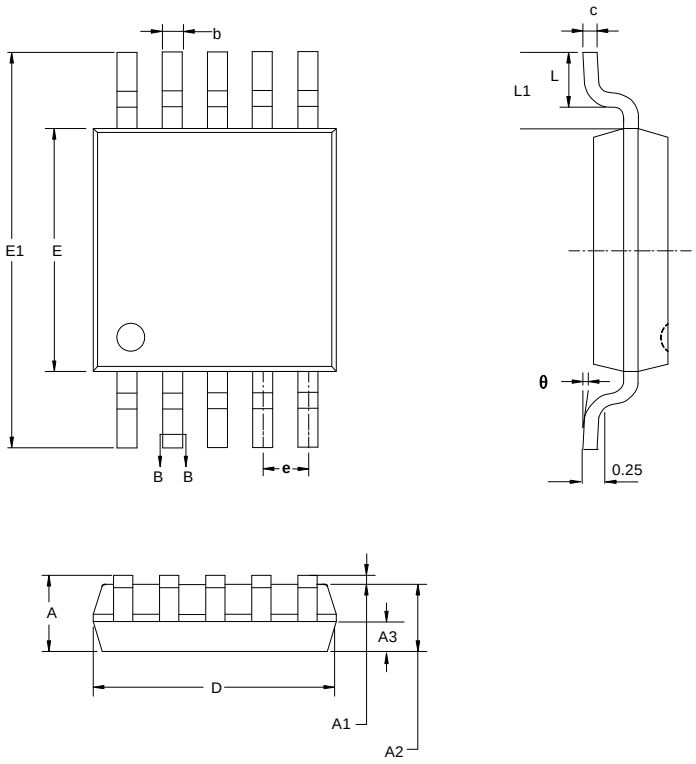
MSOP10



symbol	Size (mm)		
	minimum	model	Max
A			1.10
A1	0.05		0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.18		0.26
c	0.15		0.19
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.70	4.90	5.10
e	0.50BSC		
L	0.40		0.70
L1	0.95REF		
θ	0°		8°

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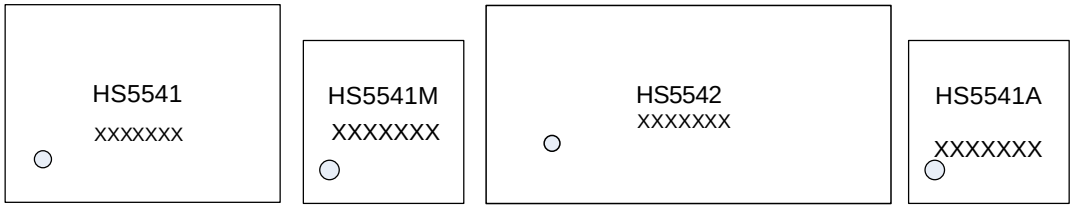
Seal and packing specification

1.Seal content introduction



Product model:HS5541、HS5541M、HS5542、HS5541A

Production lot number:XXXXXXX

2. Seal specification

Laser print, centered and Arial font.

3. Packing specification

Model number	Encapsulation form	Pieces/roll	Reel/box	Pieces/box	Box/box	Pieces/box
HS5541	SOP8	2500	1	2500	8	20000
HS5541M	MSOP8	3000	1	3000	8	24000
HS5542	SOP14	2500	1	2500	8	20000
HS5541A	MSOP10	2500	1	2500	8	20000

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statement

- Hongli Kunpeng reserves the right to change the instructions without prior notice! Customers should obtain the latest version of the information and verify that the relevant information is complete before placing an order.
- When using Hongli Kunpeng products for system design and complete machine manufacturing, the buyer has the responsibility to comply with safety standards and take appropriate safety measures to avoid personal injury or property damage caused by potential failure risks!
- Product improvement is endless, the company will be dedicated to provide customers with better products!

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MOS circuit operation precautions

Static electricity will be generated in many places, take the following preventive measures, can effectively prevent the MOS circuit due to the impact of electrostatic discharge caused by damage:

1、Use an ESD wrist strap to ground the device.

2、The device shell must be grounded.

3、Tools used during assembly must be grounded.

4、Must be packed or transported in conductor packaging or antistatic materials.

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