

FEATURES

- High Efficiency: Up to 94%
- 5A Output Current
- 4V to 15V V_{IN} Range
- Integrated Power N-Channel MOSFETs
- Adjustable Frequency 800kHz to 4MHz
- PolyPhase® Operation (Up to 12 Phases)
- Output Tracking
- 0.6V \pm 1% Reference Accuracy
- Ripple: Typical Value Less Than 10.95mV
- Current Mode Operation for Excellent Line and Load Transient Response
- Shutdown Mode Draws Less Than 15 μ A Supply Current
- Available in 24-Pin (4mm \times 4mm) QFN Package
- Adopting Soft Error Protection Technology
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

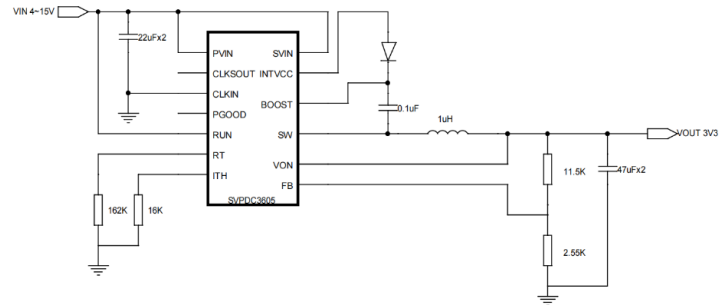
- Point of Load Power Supply
- Portable Instruments
- Distributed Power Systems
- Battery-Powered Equipment

DESCRIPTION

The HL3605 is a high efficiency, monolithic synchronous buck regulator using a phase lockable controlled on-time constant frequency, current mode architecture. PolyPhase operation allows multiple HL3605 regulators to run out of phase while using minimal input and output capacitance. The operating supply voltage range is from 15V down to 4V, making it suitable for dual lithium-ion battery inputs as well as point of load power supply applications from a 12V or 5V rail.

The operating frequency is programmable from 800kHz to 4MHz with an external resistor. The high frequency capability allows the use of small surface mount inductors. For switching noise sensitive applications, it can be externally synchronized from 800kHz to 4MHz. The PHMODE pin allows user control of the phase of the outgoing clock signal. The unique constant frequency/controlled on-time architecture is ideal for high step-down ratio applications that are operating at high frequency while demanding fast transient response. Two internal phase-lock loops synchronize the internal oscillator to the external clock and also servos the regulator on-time to lock on to either the internal clock or the external clock if it's present

TYPICAL APPLICATION

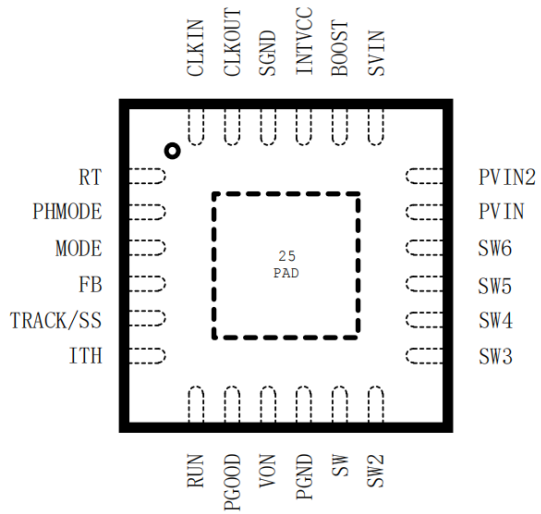


ABSOLUTE MAXIMUM RATINGS

(Note 1)

- PVIN, SVIN, SW Voltage -0.3V to 15V
- SW Transient Voltage -2V to 17.5V
- BOOST Voltage -0.3V to PVIN + INTVCC
- RUN Voltage -0.3V to 15V
- VON Voltage -0.3V to SVIN
- INTVCC Voltage -0.3V to 3.6V
- ITH, RT, CLKOUT, PGOOD Voltage -0.3V to INTVCC
- CLKIN, PHMODE, MODE Voltage -0.3V to INTVCC
- TRACK/SS, FB Voltage -0.3V to INTVCC
- Operating Temperature Range (Note 2).. -40°C to 125°C
- Junction Temperature (Note 5) 125°C
- Storage Temperature Range -65°C to 125°C

PIN CONFIGURATION



TOP VIEW

LECTRICAL CHARACTERISTICS

The denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	V_{IN} Supply Range		4		15	V
I_Q	Input DC Supply Current Active Shutdown	(Note 3) Mode = 0, $R_T = 162k$		2 220	10	mA μA
V_{FB}	Feedback Reference Voltage	COMP=1.2V (Note 4) -40°C to 85°C COMP=1.2V (Note 4) -40°C to 125°C	0.596 0.596	0.600 0.600	0.614 0.611	V V
$\Delta V_{FB(LINE)}$	Feedback Voltage Line Regulation	$V_{IN} = 4V$ to 15V, $I_{TH} = 1.2V$, -40°C to 125°C	0.01	0.08	0.3	%
$\Delta V_{FB(LOAD)}$	Feedback Voltage Load Regulation	$I_{TH} = 0.8V$ to 1.6V, -40°C to 125°C	0.059	0.17	0.32	%
I_{LIM}	Positive Inductor Valley Current Limit Negative Inductor Valley Current Limit	$V_{FB} = 0.57V$	5	6 -5	7.5	A A
V_{RUN}	Run Threshold 2 ($I_Q = 2mA$) Run Threshold 1 ($I_Q = 400\mu A$)	RUN Rising RUN Rising	1.1 0.5	1.28 0.6	1.3 0.9	V V
ΔV_{RUN}	V_{RUN} Falling, Threshold Active			100		mV
V_{INTVCC}	Internal V_{CC} Voltage	$4V < V_{IN} < 15V$	3.2	3.3	3.5	V
OV	Output Overvoltage PGOOD Upper Threshold	V_{FB} Rising	5	8	11	%
UV	Output Undervoltage PGOOD Lower Threshold	V_{FB} Falling	-13	-10	-7	%
R_{PGOOD}	PGOOD Pull-Down Resistance	1mA Load		25		Ω
I_{PGOOD}	PGOOD Leakage	$0.54V < V_{FB} < 0.66V$		31.6		μA
$I_{TRACK/SS}$	TRACK Pull-Up Current			2.2	4	μA
f_{OSC}	Oscillator Frequency	$R_T = 162k$		1		MHz
CLKIN	CLKIN Threshold			0.7		V
Supply Current, Low Voltage Full Load	$V_{IN} = 5V$, $V_{OUT} = 1.2V$, $I_{OUT} = 4A$		1.22	1.3		A
Ripple	$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $I_{OUT} = 4A$, $C_{OUT} = 47\mu F \times 3, 20MHz$ bandwidth			10. 95		mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The HL3605E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The HL3605I is guaranteed over the full -40°C to 125°C operating temperature range.

Note 3: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

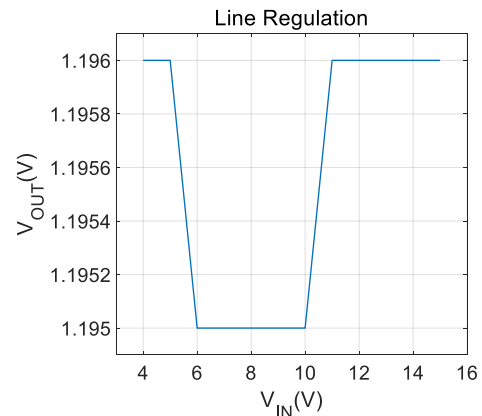
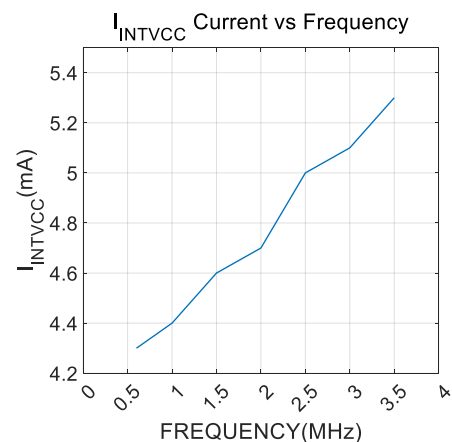
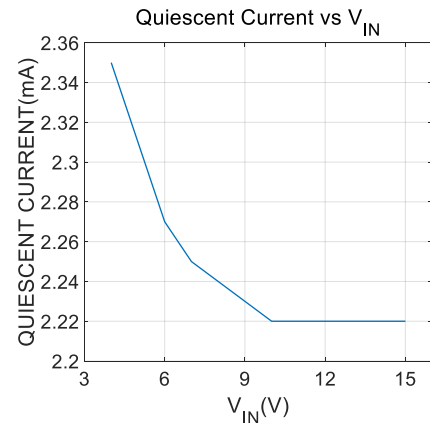
Note 4: The HL3605 is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (ITH).

Note 5: T_J is calculated from the ambient temperature T_A and power dissipation as follows: $T_J = T_A + P_D \bullet (37^\circ\text{C}/\text{W})$. See Thermal Considerations section.

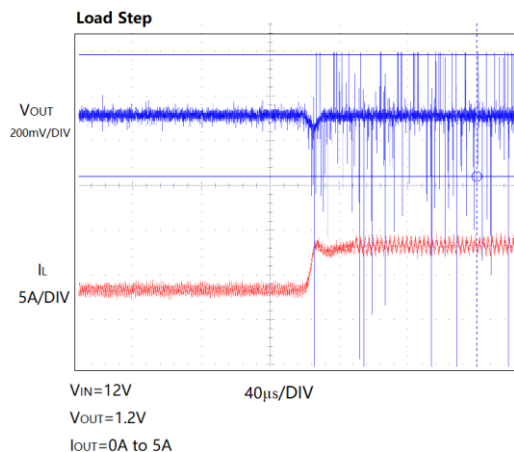
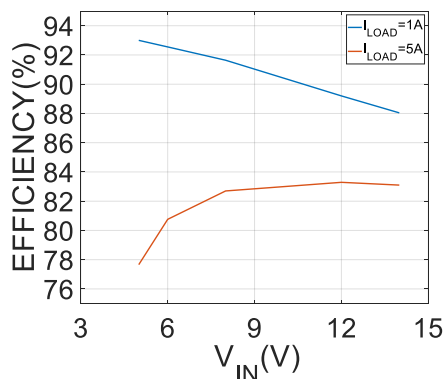
Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

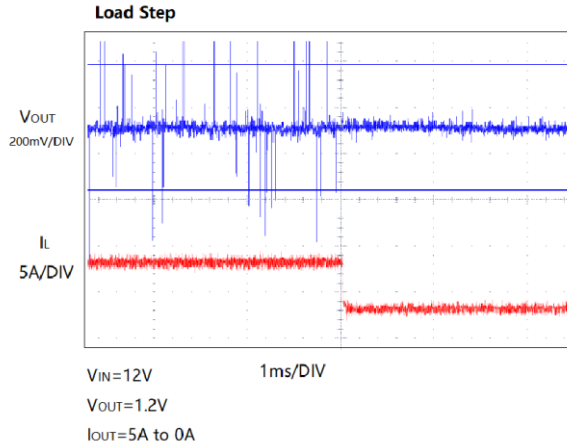
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ unless otherwise specified.

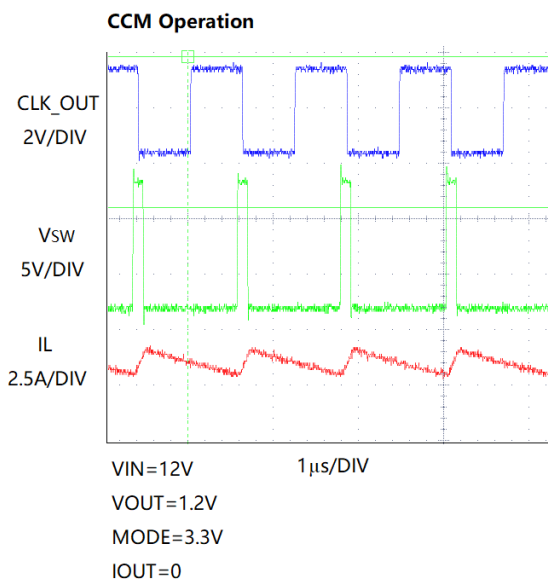
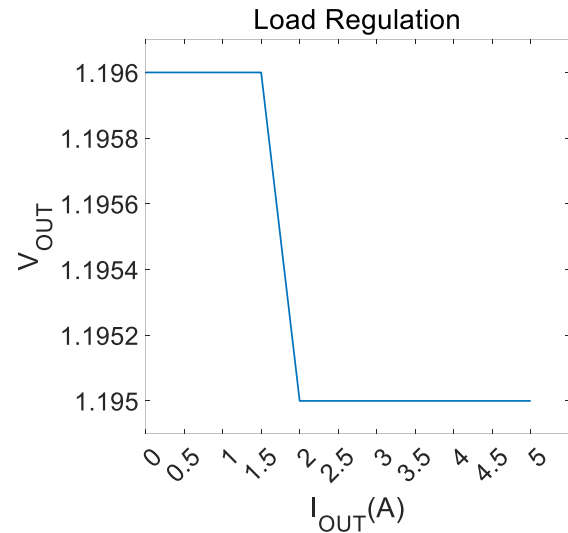
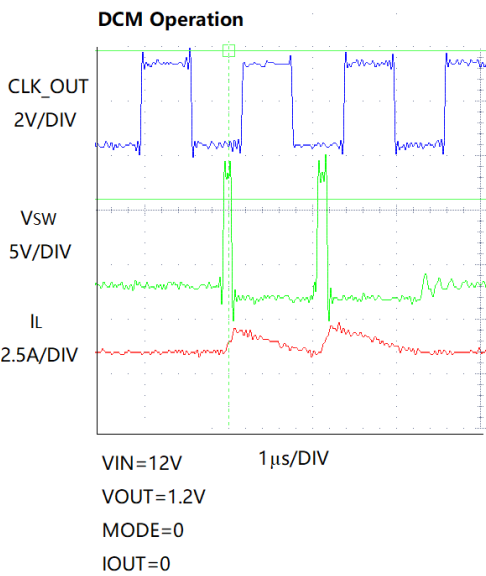
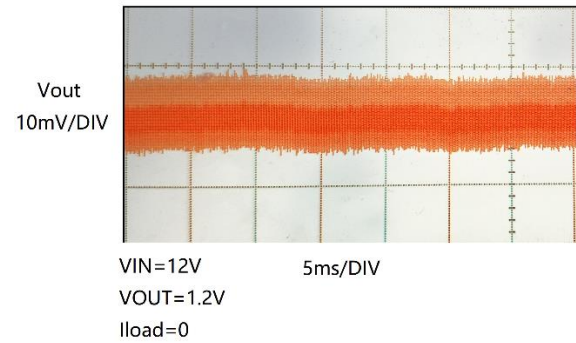


Efficiency vs V_{IN} , $V_{OUT} = 3.3\text{V}$, $F = 1\text{MHz}$





Ripple



PIN FUNCTIONS

RT (Pin 1): Oscillator Frequency Programming Pin. Connect an external resistor (between 200k to 40k) from RT to SGND to program the frequency from 800kHz to 4MHz. Since the synchronization range is $\pm 30\%$ of set frequency, be sure that the set frequency is within this percentage range of the external clock to ensure frequency lock.

PHMODE (Pin 2): Control Input to Phase Selector. Determines the phase relationship between internal oscillator and CLKOUT. Tie it to INTVCC for 2-phase operation, tie it to SGND for 3-phase operation, and tie it to INTVCC/2 for 4-phase operation.

MODE (Pin 3): Operation Mode Select. Tie this pin to INTVCC to force continuous synchronous operation at all output loads. Tying it to SGND enables discontinuous mode operation at light loads. Do not float this pin.

FB (Pin 4): Output Feedback Voltage. Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. This pin is normally connected to a resistive divider from the

output voltage.

TRACK/SS (Pin 5): Output Tracking and Soft-Start Pin. Allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, instead it servos the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 2 μ A pull-up current from INTVCC on this pin, so putting a capacitor here provides soft-start function.

ITH (Pin 6): Error Amplifier Output and Switching Regulator Compensation Point. The current comparator's trip threshold is linearly proportional to this voltage, whose normal range is from 0.3V to 1.8V. Tying this pin to INTVCC activates internal compensation and output voltage positioning, raising VOUT to 1.5% higher than the nominal value at IOU = 0 and 1.5% lower at IOU = 5A.

RUN (Pin 7): Run Control Input. Enables chip operation by tying RUN above 1.2V. Tying it below 1.1V shuts down the part.

PGOOD (Pin 8): Output Power Good with Open-Drain Logic. PGOOD is pulled to ground when the voltage on the FB pin is not within $\pm 10\%$ of the internal 0.6V reference.

VON (Pin 9): On-Time Voltage Input. Voltage trip point for the on-time comparator. Tying this pin to the output voltage makes the on-time proportional to VOUT and keeps the switching frequency constant at different VOUT. However, when VON is <0.6V or >6V, then switching frequency will no longer remain constant.

PGND (Pin 10, Exposed Pad Pin 25): Power Ground. Return path of internal power MOSFETs. Connect this pin to the negative terminals of the input capacitor and output capacitor. The exposed pad must be soldered to the PCB ground for electrical contact and rated thermal performance.

SW (Pins 11 to 16): Switch Node Connection to External Inductor. Voltage swing of SW is from a diode voltage drop below ground to PVIN.

PVIN (Pins 17, 18): Power VIN. Input voltage to the on-chip power MOSFETs.

SVIN (Pin 19): Signal VIN. Filtered input voltage to the on-chip 3.3V regulator. Connect a (1 Ω to 10 Ω) resistor between SVIN and PVIN and bypass to GND with a 0.1 μ F capacitor.

BOOST (Pin 20): Boosted Floating Driver Supply for Internal Top Power MOSFET. The (+) terminal of the bootstrap capacitor connects here. This pin swings from a diode voltage drop below INTVCC up to PVIN + INTVCC.

INTVCC (Pin 21): Internal 3.3V Regulator Output. The internal power drivers and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 1 μ F low ESR ceramic capacitor.

SGND (Pin 22): Signal Ground Connection.

CLKOUT (Pin 23): Output Clock Signal for PolyPhase Operation. The phase of CLKOUT with respect to CLKIN is determined by the state of the PHMODE pin. CLKOUT's peak-to-peak amplitude is INTVCC to GND.

CLKIN (Pin 24): External Synchronization Input to Phase Detector. This pin is internally terminated to SGND with 20k. The phase-locked loop will force the top power NMOS's turn on signal to be synchronized with the rising edge of the CLKIN signal.

Main Control Loop

The HL3605 is a current mode monolithic step-down regulator. In normal operation, the internal top power MOSFET is turned on for a fixed interval determined by a one-shot timer, OST. When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator, ICMP, trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage drop across the bottom power MOSFET's VDS. The voltage on the ITH pin sets the comparator threshold corresponding to the inductor valley current. The error amplifier, EA, adjusts this ITH voltage by comparing the feedback signal, VFB, from the output voltage with that of an internal 0.6V reference. If the load current increases, it causes a drop in the feedback voltage relative to the internal reference. The ITH voltage then rises until the average inductor current matches that of the load current. At low load current, the inductor current can drop to zero and become negative. This is detected by current reversal comparator, IREV, which then shuts off the bottom power MOSFET, resulting in discontinuous operation. Both power MOSFETs will remain off with the output capacitor supplying the load current until the ITH voltage rises above the zero current level (0.6V) to initiate another cycle. Discontinuous mode operation is disabled by tying the MODE pin to

INTVCC, which forces continuous synchronous operation regardless of output load.

The operating frequency is determined by the value of the RT resistor, which programs the current for the internal oscillator. An internal phase-lock loop servos the oscillator frequency to an external clock signal if one is present on the CLKIN pin. Another internal phase-lock loop servos the switching regulator on-time to track the internal oscillator to force constant switching frequency. Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage, VFB, exits a $\pm 10\%$ window around the regulation point. Continuous operation is forced during OV and UV condition except during start-up when the TRACK pin is ramping up to 0.6V.

Foldback current limiting is provided if the output is shorted to ground. As VFB drops to zero, the maximum sense voltage allowed across the bottom power MOSFET is lowered to approximately 40% of the original value to reduce the inductor valley current.

Pulling the RUN pin to ground forces the HL3605 into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Bringing the RUN pin above 0.7V turns on the internal reference only, while still keeping the power MOSFETs off. Further increasing the RUN voltage above 1.2V turns on the entire chip.

INTV_{CC} Regulator

An internal low dropout (LDO) regulator produces the 3.3V supply that powers the drivers and the internal bias circuitry. The INTVCC can supply up to 100mA RMS and must be bypassed to ground with a minimum of 1 μ F ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Connecting a load to the INTVCC pin is not recommended since it will further push the LDO into its RMS current rating while increasing power dissipation and die temperature.

V_{IN} Overvoltage Protection

In order to protect the internal power MOSFET

devices against transient voltage spikes, the HL3605 constantly monitors the VIN pin for an overvoltage condition. When VIN rises above 17V, the regulator suspends operation by shutting off both power MOSFETs. Once VIN drops below 15V, the regulator immediately resumes normal operation. The regulator does not execute its soft-start function when exiting an overvoltage condition.

PV_{IN}/SV_{IN} Voltage Differential

SVIN should be tied to PVIN with a low pass filter of 1 Ω to 10 Ω and 0.1 μ F. For applications where PVIN and SVIN are tied to vastly different voltage potentials, though the output voltage will remain in regulation, there will be an offset in the internal on-time generator such that if SVIN is different than PVIN by more than 50% of the PVIN voltage, the resulting switching frequency will deviate from the frequency programmed by the RT resistor and/or the external clock synchronization frequency. In such applications, in order to return the switching frequency back to the original desired frequency, RT resistor value can be adjusted accordingly. However, the better alternative is to tie the VON pin to a voltage different than that of VOUT in order to negate the offset of the VIN differential. For instance, if SVIN is 6V and PVIN is 12V, the resulting switching frequency may be slower than what's programmed by the RT resistor. Tying the VON pin to a voltage half of VOUT will negate the VIN offset and return the switching frequency back to normal.

Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.6V \cdot (1 + R_2/R_1)$$

The resistive divider allows the VFB pin to sense a fraction of the output voltage as shown in Figure 1.

Programming Switching Frequency

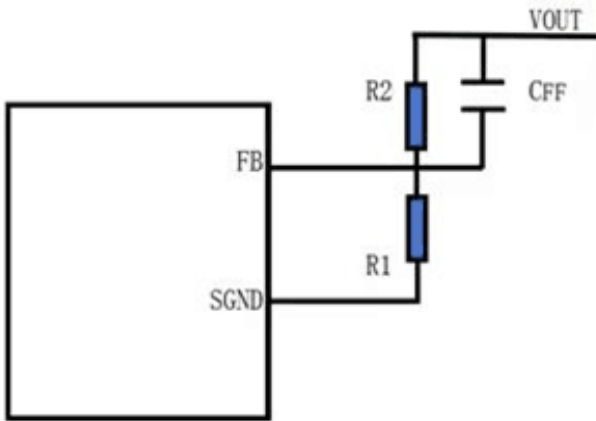


Figure 1 Setting the Output Voltage

Connecting a resistor from the RT pin to SGND programs the switching frequency from 800kHz to 4MHz according to the following formula:

$$Frequency(Hz) = \frac{1.6e^{11}}{R_T(\Omega)}$$

The internal PLL has a synchronization range of $\pm 30\%$ around its programmed frequency. Therefore, during external clock synchronization be sure that the external clock frequency is within this $\pm 30\%$ range of the RT programmed frequency.

Output Voltage Tracking and Soft-Start

The HL3605 allows the user to program its output voltage ramp rate by means of the TRACK/SS pin. An internal $2\mu A$ pulls up the TRACK/SS pin to INTVCC. Putting an external capacitor on TRACK/SS enables soft starting the output to prevent current surge on the input supply. For output tracking applications, TRACK/SS can be externally driven by another voltage source. From 0V to 0.6V, the TRACK/SS voltage will override the internal 0.6V reference input to the error amplifier, thus regulating the feedback voltage to that of TRACK/SS pins. During this start-up time, the HL3605 will operate in discontinuous mode. When TRACK/SS is above 0.6V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage.

Output Power Good

When the HL3605's output voltage is within the $\pm 10\%$ window of the regulation point, which is reflected back as a VFB voltage in the range of 0.54V to 0.66V, the output voltage is good and the PGOOD pin is pulled high with an external resistor.

Otherwise, an internal open-drain pull-down device (12Ω) will pull the PGOOD pin low. To prevent unwanted PGOOD glitches during transients or dynamic

VOUT changes, the HL3605's PGOOD falling edge includes a blanking delay of approximately 52 switching cycles.

Multiphase Operation

For output loads that demand more than 5A of current, multiple HL3605s can be cascaded to run out of phase to provide more output current. The CLKIN pin allows the HL3605 to synchronize to an external clock ($\pm 50\%$ of frequency programmed by RT) and the internal phase-locked-loop allows the HL3605 to lock onto CLKIN's phase as well. The CLKOUT signal can be connected to the CLKIN pin of the following HL3605 stage to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to INTVCC, SGND or INTVCC/2 generates a phase difference (between CLKIN and CLKOUT) of 180 degrees, 120 degrees, or 90 degrees respectively, which corresponds to 2-phase, 3-phase or 4-phase operation. A total of 12 phases can be cascaded to run simultaneously out of phase with respect to each other by programming the PHMODE pin of each HL3605 to different levels.

Internal/External ITH Compensation

During single phase operation, the user can simplify the loop compensation by tying the ITH pin to INTVCC to enable internal compensation. This connects an internal 30k resistor in series with a 40pF capacitor to the output of the error amplifier (internal ITH compensation point) while also activating output voltage positioning such that the output voltage will be 1.5% above regulation at no load and 1.5% below regulation at full load. This is a trade-off for simplicity instead of OPTILOOP® optimization, where ITH components are external and are selected to optimize the loop transient response with minimum output capacitance.

Minimum Off-Time and Minimum On-Time Considerations

The minimum off-time, $t_{OFF(MIN)}$, is the smallest amount of time that the HL3605 is capable of turning on the bottom power MOSFET, tripping the

current comparator and turning the power MOSFET back off. This time is generally about 70ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its "on" state. This time is typically 40ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$DC_{MIN} = f \cdot t_{ON(MIN)}$$

where $t_{ON(MIN)}$ is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint. In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. This is an acceptable result in many applications, so this constraint may not be of critical importance in most cases. High switching frequencies may be used in the design without any fear of severe consequences. As the sections on inductor and capacitor selection show, high switching frequencies allow the use of smaller board components, thus reducing the size of the application circuit.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum R_{MS} current should be used. The maximum R_{MS} current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} \cong I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT} , is determined by:

$$\Delta V_{OUT} < \Delta I_L \left(\frac{1}{8fC_{OUT}} + ESR \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints. Their relatively low value of bulk capacitance may require multiples in parallel.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric

formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, VDROOP, is usually about 2 to 3 times the linear drop of the first cycle. Thus, a good place to start with the output capacitor value is approximately:

$$C_{OUT} \approx F \times \frac{\Delta I_{OUT}}{f_o \times V_{FALL}}$$

More capacitance may be required depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 22µF ceramic capacitor is usually enough for these conditions. Place this input capacitor as close to the PV_{IN} pins as possible.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{f \times L} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 2.5A. This is especially important at low V_{OUT} operation where V_{OUT} is 1.8V or below. Care must be given to choose an inductance value that will generate a big enough current ripple (1.5A to 2.5A) so that the chip's valley current comparator has enough signal-to-noise ratio to force constant switching frequency. Meanwhile, also note that the largest ripple current occurs at the

highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum.

However, the inductor ripple current must not be so large that its valley current level (–ΔI_L/2) can exceed the negative current limit, which can be as low as –3.5A. If the negative current limit is exceeded in forced continuous mode of operation, V_{OUT} can get charged to above the regulation level until the inductor current no longer exceeds the negative current limit. In such instances, choose a larger inductor value to reduce the inductor ripple current. The alternative is to reduce the RT resistor value to increase the switching frequency in order to reduce the inductor ripple current.

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Toko, Vishay, NEC/Tokin, Cooper, TDK and Würth Elektronik. Refer to Table 1 for more details.

Checking Transient Response

The OPTI-LOOP compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the ITH pin not only allows optimization of the control loop

behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The ITH external components shown in the circuit on the first page of this data sheet provides an adequate starting point for most applications. The series R-C filter sets the dominant pole zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \cdot ESR$, where ESR is the effective series resistance of C_{OUT} . ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with the R and the bandwidth of the loop increases with decreasing C. If R is increased by the same factor that C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, a feedforward capacitor, C_{FF} , can be added to improve the high frequency response, as shown in Figure 1. Capacitor C_{FF} provides phase lead by creating a high frequency zero with R2 which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology

Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>10µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT} , causing a rapid drop in V_{OUT} . No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection and soft-starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + \dots)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in HL3605 circuits: 1) I^2R losses, 2) switching and biasing losses, 3) other losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW} , and external inductor, R_L . In continuous mode, the average output current flows through inductor L but is “chopped” between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

$$I^2R \text{ losses} = I_{OUT}^2 (R_{SW} + R_L)$$

2. The $INTV_{CC}$ current is the sum of the power MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger

than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. Since INTV_{CC} is a low dropout regulator output powered by V_{IN}, its power loss equals:

$$P_{LDO} = V_{IN} I_{INTVCC}$$

Refer to the I_{INTVCC} vs Frequency curve in the Typical Performance Characteristics for typical INTV_{CC} current at various frequencies.

- Other “hidden” losses such as transition loss and cop- per trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these “system” level losses in the design of a system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The HL3605 internal power devices switch quickly enough that these losses are not signifi- cant compared to other sources. Other losses including diode conduction losses during dead-time and inductor core losses which generally account for less than 2% total additional loss.

Thermal Considerations

In a majority of applications, the HL3605 does not dissipate much heat due to its high efficiency and low thermal resistance of its exposed-back QFN package. However, in applications where the HL3605 is running at high ambient temperature, high V_{IN}, high switching frequency and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, both power switches will be turned off until the temperature drops about 15°C cooler.

To avoid the HL3605 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \theta_{JA}$$

As an example, consider the case when the HL3605 is used in applications where V_{IN} = 12V, I_{OUT} = 5A, f = 1MHz, V_{OUT} = 1.8V. The equivalent power MOSFET resistance R_{SW} is:

$$R_{SW} = R_{DS(ON)TOP} \cdot \frac{V_{OUT}}{V_{IN}} + R_{DS(ON)BOT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The V_{IN} current during 1MHz force continuous operation

with no load is about 11mA, which includes switching and internal biasing current loss, transition loss, inductor core loss and other losses in the application. Therefore, the total power dissipated by the part is:

$$P_D = I_{OUT}^2 R_{SW} + V_{IN} I_{VIN} (NO\ Load)$$

The QFN 4mm × 4mm package junction-to-ambient thermal resistance, θ_{JA} , is around 37°C/W. Therefore, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

$$T_J = P_D \cdot 37^\circ C/W + 25^\circ C$$

Remembering that the above junction temperature is obtained from an R_{DS(ON)} at 25°C, we might recalculate the junction temperature based on a higher R_{DS(ON)} since it increases with temperature. Redoing the calculation assuming that R_{SW} increased 15% at 67°C yields a new junction temperature of 72°C. If the application calls for a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow. Figure 2 is a temperature derating curve based on the demo board.

Junction Temperature Measurement

The junction-to-ambient thermal resistance will vary depending on the size and amount of heat sinking copper on the PCB board where the part is mounted, as well as the amount of air flow on the device. One of the ways to measure the junction temperature directly is to use the internal junction diode on one of the pins (PGOOD) to measure its diode voltage change based on ambient temperature change. First remove any external passive component on the PGOOD pin, then pull out 100µA from the PGOOD pin to turn on its internal junction diode and bias the PGOOD pin to a negative voltage. With no output current load, measure the PGOOD voltage at an ambient temperature of 25°C, 75°C and 125°C to establish a slope relationship between the delta voltage on PGOOD and delta ambient temperature. Once this slope is established, then the junction temperature rise can be measured as a function of power loss in the package with corresponding output load current. Keep in mind that doing so will violate absolute maximum voltage ratings on the PGOOD pin, however, with the limited current, no damage will result.

Board Layout Considerations

When laying out the printed circuit board, the following

checklist should be used to ensure proper operation of the HL3605 (refer to Figure 3). Check the following in your layout:

1. Do the capacitors C_{IN} connect to the power PV_{IN} and power PGND as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.
2. Are C_{OUT} and L1 closely connected? The (-) plate of C_{OUT} returns current to PGND and the (-) plate of C_{IN} .
3. The resistive divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and a ground line terminated near SGND. The feedback signal V_{FB} should be routed away from noisy components and traces, such as the SW line, and its traces should be minimized. Keep R1 and R2 close to the IC.
4. Solder the Exposed Pad (Pin 25) on the bottom of the package to the PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the HL3605.
5. Keep sensitive components away from the SW pin. The R_T resistor, the compensation capacitor C_C and C_{ITH} and all the resistors R1, R3 and R_C , and the $INTV_{CC}$
6. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small-signal components returning to the SGND pin which is then connected to the PGND pin at the negative terminal of the output capacitor, C_{OUT} .

Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. These copper areas should be connected to PGND.

Design Example

As a design example, consider using the HL3605 in an application with the following specifications:

$V_{IN} = 10.8V$ to $13.2V$, $V_{OUT} = 1.8V$, $I_{OUT(MAX)} = 5A$,
 $I_{OUT(MIN)} = 500mA$, $f = 2MHz$

Because efficiency is important at both high and low load current, discontinuous mode operation will be utilized. First select from the characteristic curves the correct R_T resistor value for 2MHz switching frequency. Based on that R_T should be 80.6k. Then calculate the inductor value for about 50% ripple current at maximum V_{IN} :

$$L = \left(\frac{V_{OUT}}{f \cdot I_{OUT}} \right) \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

The nearest standard value inductor would be 0.33μH.

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, two 47μF ceramic capacitors will be used.

$$L = \left(\frac{V_{OUT}}{f \cdot I_{OUT}} \right) \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

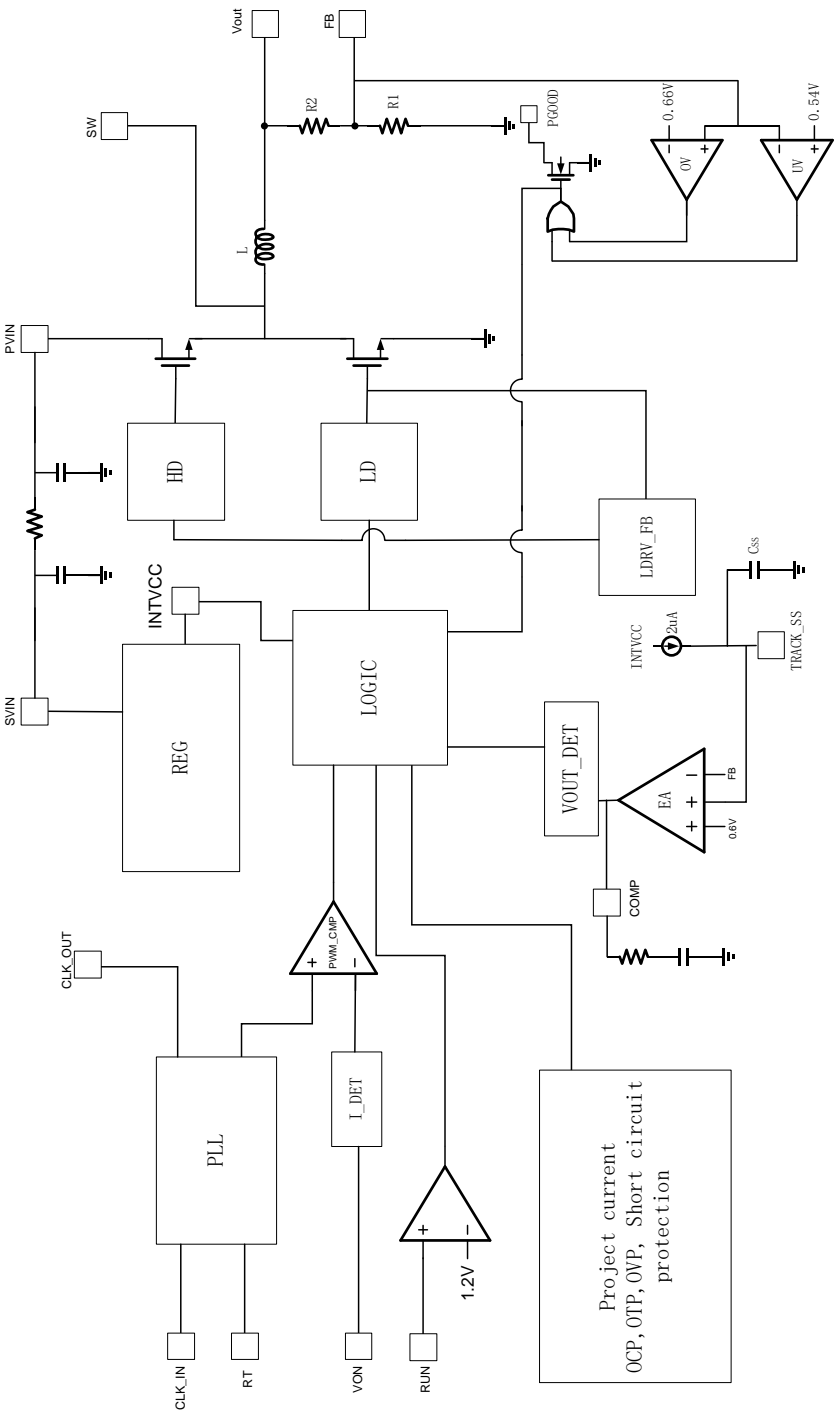
The nearest standard value inductor would be 0.33μH. C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, two 47μF ceramic capacitors will be used.

C_{IN} should be sized for a maximum current rating of:

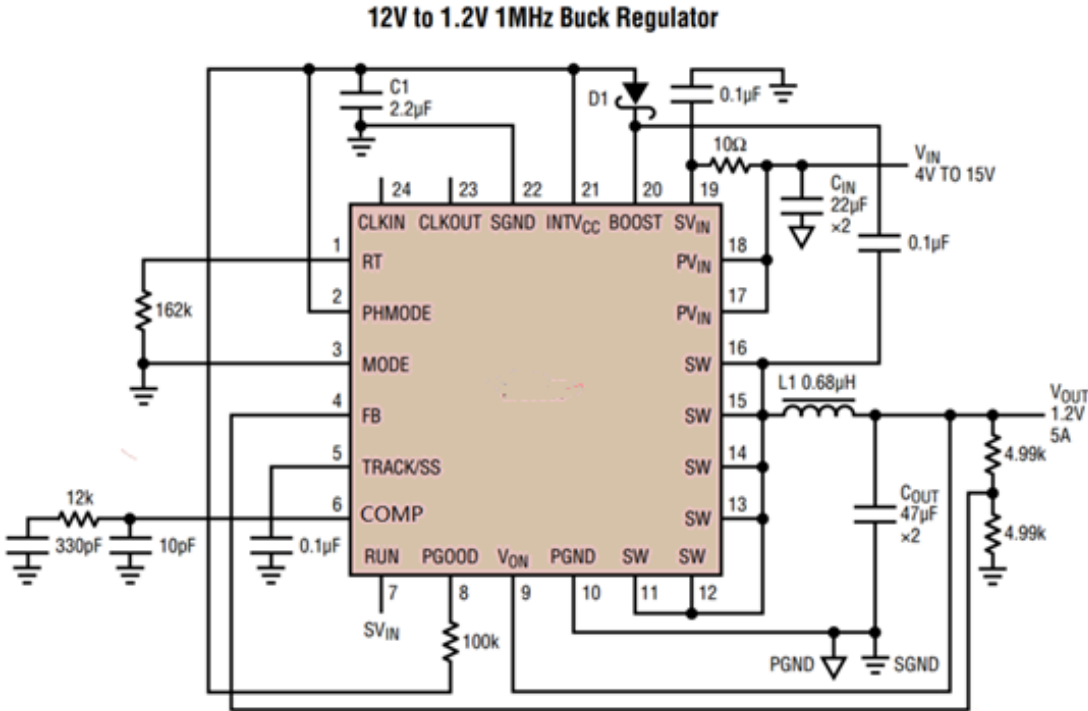
$$I_{RMS} = I_{OUT} \left(\frac{V_{OUT}}{V_{IN}} \right) \left(\frac{V_{IN}}{V_{OUT}} \right)^{1/2}$$

Decoupling the PV_{IN} pins with two 22μF ceramic capacitors is adequate for most application

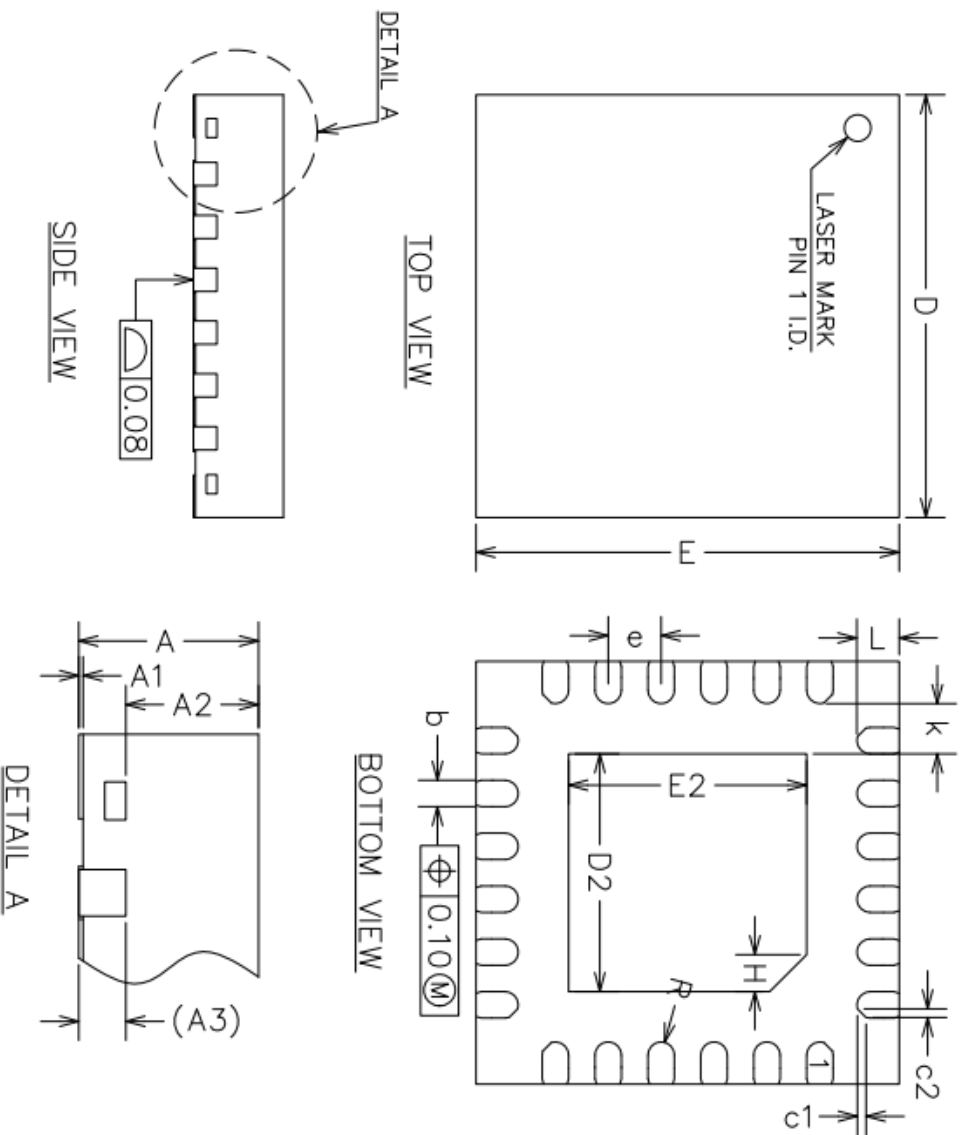
Functional Block Diagram



TYPICAL APPLICATION



ENCAPSULATION



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.15	2.25	2.35
E2	2.15	2.25	2.35
e	0.40	0.50	0.60
H	0.35REF		
K	0.30	-	-
L	0.35	0.40	0.45
R	0.09	-	-
c1	-	0.08	-
c2	-	0.08	-

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDRAD
MO-220 VGGD-8.DO NOT INCLUDE MOLD FLASH-
OR PROTRUSION.