



16-bit 80MSPS dual-channel Analog-to-Digital Converter (ADC)

1 Main features:

- ◆ Conversion bits: 16 bits
- ◆ Clock frequency: 80 MSPS
- ◆ Supply voltage: 1.8V
- ◆ Power consumption: 245 mW/CH
- ◆ Data interface: CMOS/LVDS interface
- ◆ SFDR: 93dBc@9.7MHz input
- ◆ SNR: 79dBFS@9.7MHz input
- ◆ Optional in-film jitter
- ◆ Programmable ADC internal reference voltage source
- ◆ 1 to 8 integer input clock divider
- ◆ Encapsulation: QFN64

2. Typical applications

- ◆ Wireless communication system
- ◆ Intelligent antenna system
- ◆ Software radio
- ◆ Broadband data application
- ◆ Medical ultrasound equipment
- ◆ Radar and aviation systems

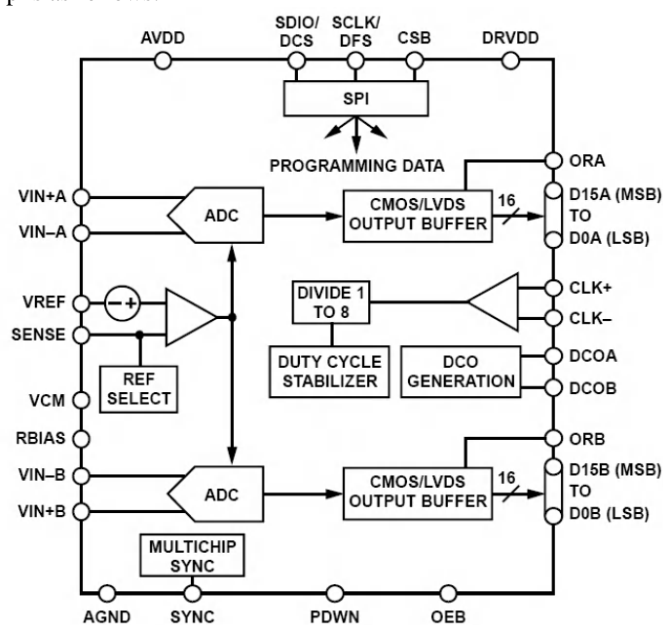
3 Product Description

The chip is a 16-bit, 80 MSPS dual-channel ADC designed for communication applications requiring high performance, low cost, and small size. The ADC core uses a multi-level, differential pipeline architecture and integrates output error correction logic. The front-end wideband differential sampling and holding circuit allows users to flexibly select various input ranges. The reference voltage circuit is integrated in the chip.

5 Compared with similar foreign products

	precision	Clock frequency	Data port	CH power consumption	SNR	SFDR	Encapsulation form
AD9269 (ADI)	16Bit	80MHz	CMOS	100mW@80 MSPS	77.6dBFS@ 9.7MHz	93dBc@70 MHz	LFCSP64
BLAD16D80 (Beiling)	16Bit	80MHz	CMOS/LVDS	238mW@80 MSPS	77.5dBFS@ 10MHz	90dBc@70 MHz	QFN64
MT9268	16Bit	80MHz	CMOS/LVDS	240mW@8 0MSPS	79dBFS@9. 7MHz	93dBc@70 MHz	QFN64

The chip has a clock duty ratio regulator, which can compensate the fluctuation of ADC clock duty ratio and ensure the output performance of the converter. The output of the chip is CMOS signal or LVDS signal. The chip has a power saving mode to reduce power consumption. The chip implements various configurations through the three-wire SPI interface. The chip adopts QFN64 package and is compatible with foreign products AD9269 pin, which can be replaced. The internal structure block diagram of the chip is as follows:



4 Product Highlights

- ◆ Optional on-chip jitter option improves small-signal SFDR performance.
- ◆ Proprietary differential inputs maintain excellent SNR at 300 MHz input frequencies.
- ◆ Standard serial port configuration: output data format, clock DCS enable, power saving mode, test mode, reference voltage value, etc.