16/14/12 Bit 500MSPS Dual channel digital-to-analog Converter (DAC)

1 Main features:

◆ Conversion bits: 16/14/12 bits

◆ Clock frequency: 500 MSPS

◆ Output current: 8~ 32 mA

◆ Supply voltage: 1.8V, 3.3V

◆ Power consumption: 440 mW

◆ Data interface: LVDS double-ended or interleaved single-ended interface with an on-chip 100Ω termination resistor

◆ SFDR 80dBc@50MHzoutput

◆ IMD3 85dBc@50MHzoutput

◆ NSD -162dBm/Hz @50MHzoutput

◆ Internal auxiliary 10-bit current DAC with source/draw current capability for eliminating external offset zeros

◆ Encapsulation：QFN72

2. Typical applications

◆ Wireless communication WCDMA CDMA200 0 TD-SCDMA WiMAX

◆ Broadband point-to-point communication

◆ RF signal generator

◆ Arbitrary waveform generator

◆ Instrumentation and automatic test equipment

◆ Radar and aviation systems

3 Product Description

This series of chips is a 16/14/12-bit, 500 MSPS dual-channel DAC. It includes: external data receiving circuit, clock receiving circuit, digital decoding circuit, voltage reference circuit, DAC core circuit and so on

The main module. The DAC core adopts the current rudder structure, and provides two operating modes: baseband mode and mixing mode. The chip is suitable for the application of direct frequency conversion transmission and has the function of gain and offset compensation. In the mixing output mode, the chip can shift the signal energy from the fundamental frequency to the mirror frequency, so that the analog output synthesis can be realized in the frequency range higher than Nyquist. The chip uses LVDS interface to realize data input, and ensures correct data reception through internal data receiving timing control circuit. The output current of the chip can be adjusted in the range of 8mA to 32mA. The chip is powered by 1.8V and 3. 3V power supplies. The chip realizes the configuration function by serial peripheral interface SPI interface. Chip adopts QFN72 package, and foreign products

The AD9783/81/80 series products are pin compatible and can be replaced. The internal structure block diagram of the chip is as follows:
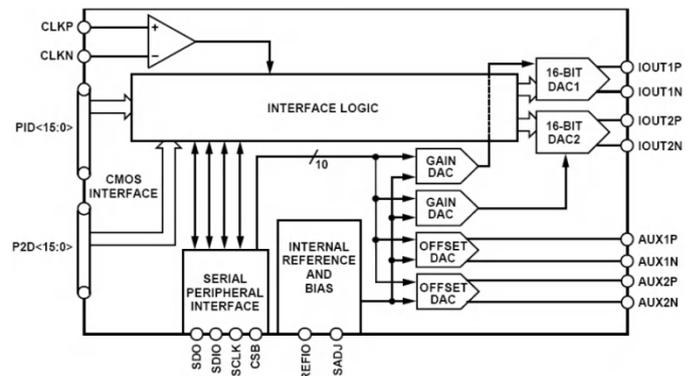
4 Product Highlights

◆ Low noise and low intermodulation distortion (IMD) to synthesize high quality broadband signals.

◆ Special switching output structure to enhance dynamic performance.

◆ Programmable current outputs with dual auxiliary Dacs provide both flexibility and enhanced system functionality.

5 Compared with similar foreign products

	precision	Clock frequency	Data port	Power dissipation	Output current	SFDR	Encapsulation form
AD9783 （ADI）	16Bit	500MHz	LVDS double-ended or interlaced Type single-ended interface	440mW@500MSPS	8.6 - 31.7mA	66dBc@120 MHz	LFCSP72
AD9752 （ADI）	12Bit	125MSPS	two-port CMOS	185mW@125MSPS	2 - 20mA	55dBc@40 MHz	TSSOP28
HL9783	16Bit	500MHz	LVDS double-ended or interlaced Type single-ended interface	440mW@500MSPS	8 - 32mA	67dBc@100 MHz	QFN72