



14-bit 2.5GSPS Single-channel Digital-to-Analog Converter (DAC)

1 Main features:

- ◆ Converted bits: 14 bits
- ◆ Clock frequency: 2.5 GSPS
- ◆ Output current: 8 - 32 mA
- ◆ Supply voltage: 1.8V, 3.3V
- ◆ Power consumption: 1.2W@2.5GSPS
- ◆ Data interface: Dual-port LVDS data interface
- ◆ SFDR: 66 dBc @100 MHz output
- ◆ IMD3: 90 dBc @ 100 MHz output
- ◆ NSD: -165 dBm/Hz @ 100 MHz output
- ◆ Encapsulation: FCBGA160

2 Typical application

- ◆ Broadband communication system
- ◆ Television transmission system
- ◆ Cellular communications infrastructure
- ◆ Point-to-point wireless system
- ◆ Instrumentation and automatic test equipment
- ◆ Radar and aviation systems

3 Product description

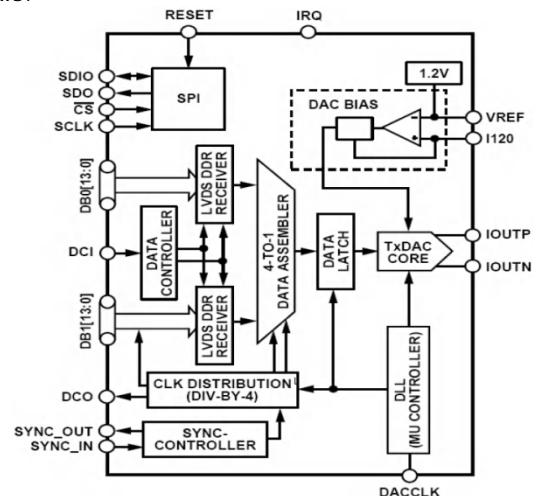
This product is a 14-bit 2.5GSPS single-channel DAC chip, which includes: external data receiving circuit, clock receiving circuit, high-speed digital decoding circuit, multi-chip synchronization circuit, voltage reference circuit, DAC core circuit and other main modules. The DAC core adopts current rudder junction

It also provides two working modes: baseband mode and mixing mode. In baseband mode, the chip can output high-quality analog signals in the first Nyquist frequency range. In mixing mode, the chip can output high-quality analog signals in the second and third Nyquist frequency ranges.

5 Compared with similar foreign products

	precision	Clock frequency	Data port	Power dissipation	Output current	SFDR	Encapsulation form
AD9739 (ADI)	14Bit	2.5GHz	Single port LVDS	1.1W@2.5GSPS	8.7 - 31.7mA	72dBc@100 MHz	FCBGA160
DAC904 (TI)	14Bit	165MSPS	—	170mW@ 165MSPS	0 - 20mA	64dBc@20 MHz	TSSOP28
HL9739	14Bit	2.5GHz	two-port LVDS	1.2W@2.5GSPS	8 - 32mA	66dBc@100 MHz	FCBGA160

In both modes of operation, the chip can ensure good output linearity in a wide frequency range. The chip uses two LVDS interfaces to input data, and the internal data receiving timing control circuit ensures the correct data receiving. The output current can be adjusted in the range of 8mA to 32mA, powered by a dual supply of 1.8V and 3.3V, and can be configured via the standard SPI interface. The chip adopts FCBGA160 package, which has low package parasitic effect. The internal structure block diagram of the chip is as follows:



4 Product highlights

- ◆ Low noise and intermodulation distortion (IMD) performance enable high-quality synthesis of broadband signals up to 1 GHz.
- ◆ The dual port interface with Dual Data Rate (DDR) LVDS data receiver supports a maximum conversion rate of 2500 MSPS.
- ◆ It is manufactured using CMOS process technology and uses special switching technology to enhance dynamic performance.
- ◆ The output current can be easily configured for single-ended or differential circuit topologies.