HL2030Axxxx MCU is based on 32-bit Arm® Cortex®-M0 core, supporting up to 256K bytes of flash memory and 32K bytes of SRAM, 12 timers, 1 ADC, 10 communication interfaces, 2 sets of comparators, and 3 sets of operational amplifiers.

Features:

■ Core: 32-bit Arm® Cortex®-M0 Core

- Maximum operating frequency of72MHz

■ Memory

- Supports up to 256K bytes of flash memory

- Supports up to 32K bytes of SRAM

■ Clock, Reset, and Power Management

- 1.8~3.6V supply and I/O pins

- Power-on/Power-down reset (POR/PDR), Programmable Voltage Detector (PVD)

- 4~32MHz crystal oscillator

- Embedded 8MHz RC oscillator factory calibrated (supports LSE real-time calibration)

- Embedded 14MHz RC oscillator factory calibrated (dedicated to ADC)

- Embedded calibrated 40kHz RC oscillator

- Calibrated 32kHz RTC oscillator

■ Low Power Consumption

- Sleep, stop, and standby modes

- VBAT supplies power to RTC and backup registers

■ DMA: 5-channel DMA controller

■ Debug Mode

- Serial Wire Debug (SWD)

■ I/O Ports

- Supports up to 39 multifunctional bidirectional I/O ports, all I/O ports can be mapped to external interrupts

■ Enhanced CRC Calculation Unit

■ Supports hardware division, square root module

■ 12 Timers

- 1 16-bit advanced control timer for six-channel PWM output

- 1 32-bit and seven 16-bit timers, up to four IC/OC, OCN, available for infrared control decoding

- 2 watchdog timers (independent and windowed)

- System time timer

■ 10 Communication Interfaces

- 2 I2C interfaces (support SMBus/PMBus)

- 6 USART interfaces (support ISO7816, LIN, IrDA interfaces, and modem control)

- 2 SPI interfaces, two multiplexed with I2S interfaces

■ Analog Interfaces

- 1 12-bit ADC, 1us conversion time (up to 10 input channels)

- Supports up to 3 high-speed operational amplifiers

- Supports up to 2 comparators

Contents

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1 Introduction

The contents of this datasheet include: basic configurations of the product (such as the capacity of built-in Flash and RAM, the types and quantities of peripheral modules, etc.), the number and allocation of pins, electrical characteristics, packaging information, and ordering information, etc.

2 Specification Description

Device Overview

Family		HL2030A				
Model		F8P7	K8T7	KCV7	CBT7	CCT7
Flash(K bytes)		64	64	256	128	256
SRAM(K bytes)		16	16	32	32	32
Timer	Advanced (16bit)	1	1	1	1	1
	Universal (16bit)	5	5	5	5	5
	Universal (32bit)	1	1	1	1	1
	Basic (16bit)	2	2	2	2	2
Communication Interfaces	SPI	1	2	2	2	2
	I2C	1	2	2	2	2
	USART	5	6	6	6	6
GPIO Ports		15	25	27	39	39
12-bit ADC Module (number of channels)		1(9Channel)	1(10Channel)	1(10Channel)	1(10Channel)	1(10Channel)
OPA		1	2	2	3	3
COMP		2				
DIVSQRT		Support				
CPU Frequency		72M				
Operating Voltage		1.8~3.6V				
Operating Temperature		–40~+105℃				
Packaging Form		TSSOP20	LQFP32	QFN32(4x4)	LQFP48	

Table 1 Device Features

Overview

2.1.1 ARM® Cortex® -M0 Microprocessor Platform Integrated with FLASH and SRAM

The ARM® Cortex®-M0 core is the latest generation of 32-bit core platforms developed by ARM® for small embedded systems, designed to implement convenient, low-cost solutions. This

platform provides users with excellent computational performance and rapid interrupt response while requiring only a limited number of pins and power consumption.

The ARM® Cortex®-M0 32-bit RISC processor offers excellent code efficiency, providing users with the high performance expected from the ARM core under conditions of small storage space.

All products are comprising with embedded ARM cores and keeping full compatibility with all ARM tools and software.

2.1.2 Memory

The device has the following features:

- SRAM is accessed at CPU clock speed (read/write) with no wait states and features embedded parity, generating exceptions for severe fault applications.
- Non-volatile memory is divided into two arrays:

  - 16-256KB of embedded flash, used for programs and data

  - Option bytes

  Option bytes are used for write-protecting memory (4 KB blocks) and/or readout protecting the entire memory, using the following options:

  - Level 0: No readout protection

  - Level 1: Memory readout protection; cannot read from or write to flash if debugging features are connected or if choosing to start in RAM

  - Level 2: Chip readout protection; debugging features (Cortex®- M0 serial wire) and the option to start in RAM are disabled

2.1.3 Boot Modes

At startup, the boot pins and boot selector option bits are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The bootloader is located in system memory. Flash can be reprogrammed using USART on pins PA14/PA15 or PA9/PA10 or using IIC on pins PB6/PB7.

2.1.4 CRC (Cyclic Redundancy Check) Calculation Unit

The CRC (Cyclic Redundancy Check) calculation unit is used with configurable generator polynomial values and sizes.

In other applications, CRC-based techniques are used to verify the integrity of data transmission or storage.

2.1.5 Power Management

Power Supply Scheme

- VDD = 1.8 - 3.6 V: External power for I/O and internal regulators. Externally provided through the VDD pin.
- VDDA= VDD - 3.6 V: External analog power for ADC, reset module, RC, and PLL.

The volta ge level of VDDA must be equal to or higher than VDD, and must be provided first.

Power Detector

This product integrates a Power-on Reset (POR)/Power-down Reset (PDR) circuit, which is always operational, ensuring the system works when power exceeds POR; when VDD is below the set threshold (POR/PDR), the device is in reset state, eliminating the need for an external reset circuit.

There is also a Programmable Voltage Detector (PVD) in the device, which monitors VDD/VDDA supply and compares it with the threshold VPVD, generating an interrupt when VDD is below or above the threshold VPVD. The interrupt service routine can issue warning messages or put the microcontroller into a safe mode. The PVD feature needs to be enabled by programming.

Voltage Regulator

The regulator has two operating modes and is always enabled after reset.

- Main Power (MR) is used in normal operating mode (Run).
- Low Power (LPR) can be used in stop mode, reducing power requirements.

In standby mode, it enters power-down mode. In this mode, the output of the regulator is in a high-impedance state, the core circuit is powered off, resulting in zero consumption (but the data of the registers and SRAM are lost).

- Low Power Modes

  Supports three low power modes to achieve the best trade-off between low power consumption, short startup time, and available wake-up sources:

- Sleep Mode

  In sleep mode, only the CPU is in a dormant state. When an interrupt/event occurs, all peripherals continue to operate and can wake up the CPU.

- Stop Mode

  Stop mode achieves very low power consumption while retaining the data of SRAM and registers. All clocks in the 1.1V domain are stopped, and the PLL, HSI RC, and HSE crystal oscillators are disabled. The voltage regulator can also be set to normal or low power mode. The device can be awakened from stop mode by any EXTI line. EXTI line sources can be one of the 16 external lines or the RTC.

- Standby Mode

  Standby mode is designed to achieve the lowest power consumption by turning off the internal regulator, powering down the entire 1.1V domain. The PLL, HSI RC, and HSE crystal

oscillators are also turned off. Upon entering standby mode, the data of SRAM and registers, except for those in the RTC domain and backup circuits, will be lost. The device exits standby mode when an external reset (NRST pin), IWDG reset, rising edge on the WKUP pin, or an RTC event occurs.

Note: The RTC, IWDG, and their corresponding clock sources do not stop due to entering stop or standby mode.

2.1.6 Clocks and Startup

System clock selection is performed at startup, but the internal RC 8MHz oscillator is selected as the default CPU clock at reset. An external 4-32MHz clock can be selected, in which case it is monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator. If enabled, a software interrupt is generated. Likewise, full interrupt management of the PLL clock item can be performed when necessary (e.g., when a failure occurs in the indirectly used external crystal, resonator, or oscillator).

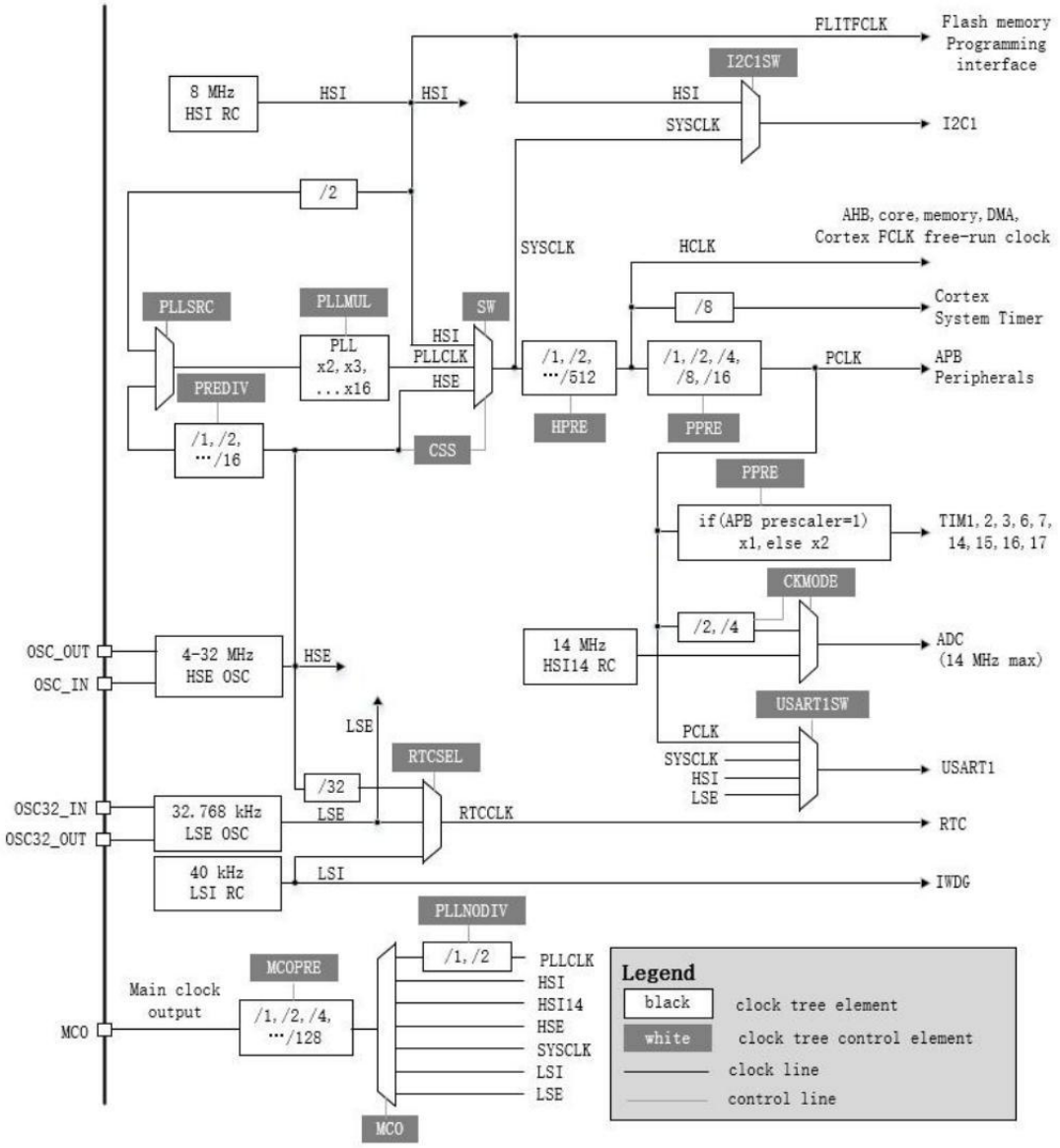


Figure 1 Clock Tree of HL2030Ax8/xB

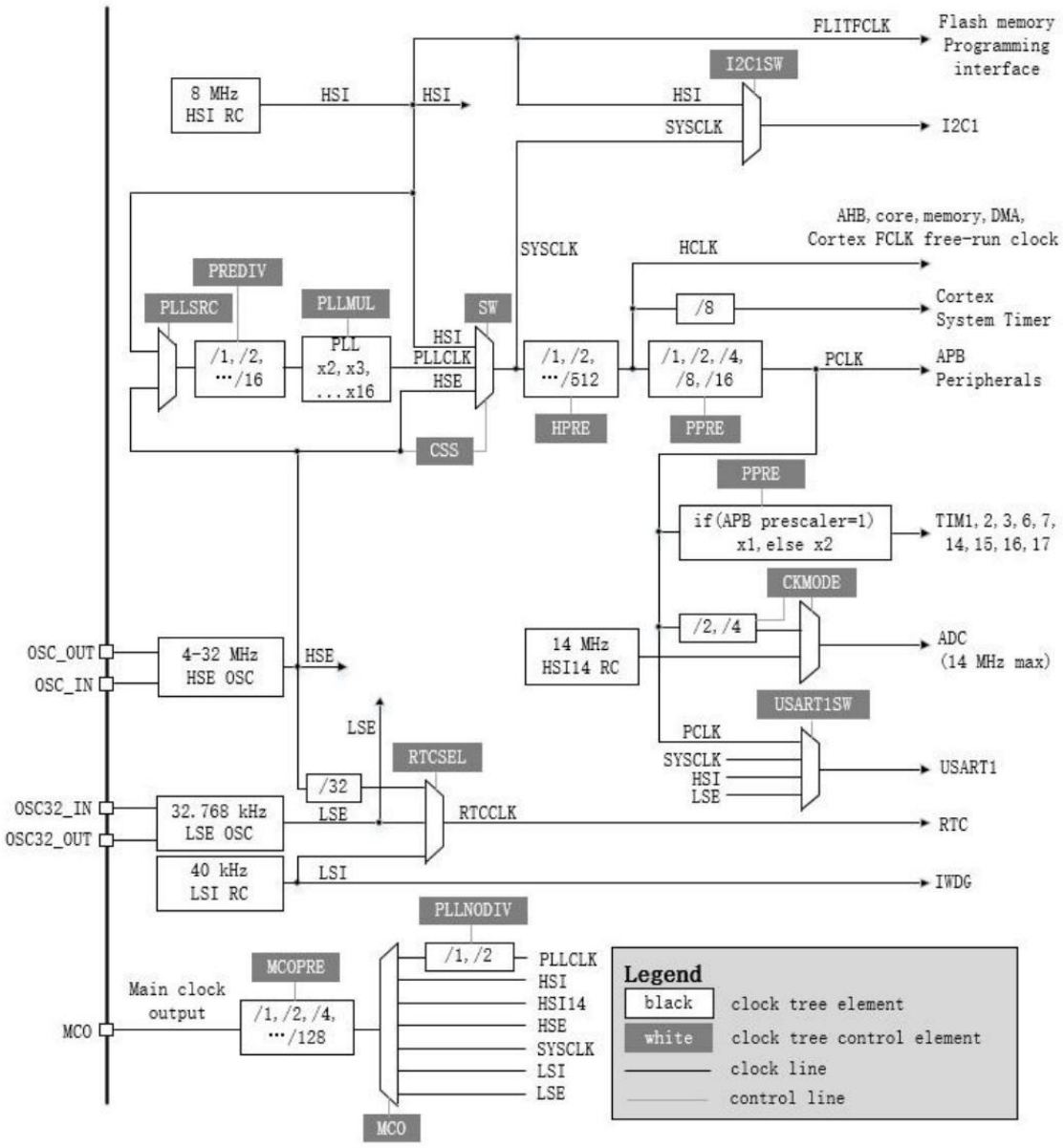


Figure 2 Clock Tree of HL2030AxC

2.1.7 GPIO

Each GPIO pin can be configured through software as output (push-pull or open-drain), input (with or without pull-up or pull-down), or peripheral alternate function. Most GPIO pins share with digital or analog alternate functions.

If needed, the I/O configuration can be locked in a specific order to avoid spurious writing to the I/O registers.

2.1.8 DMA

Supports up to 5 general-purpose DMAs that can manage data transfers from memory to memory, device to memory, and memory to device; the DMA controller supports the management of

circular buffers, avoiding interrupts generated by the controller when transfers reach the end of the buffer.

Each channel has dedicated hardware DMA request logic and can also be triggered by software for each channel; the length of the transfer, the source address, and the destination address of the transfer can all be set separately through software. DMA can be used for major peripherals: SPI, I2C, USART, advanced/general/basic timers (except TIM14), ADC, etc.

2.1.9 Interrupts and Events

Nested Interrupt Controller (NVIC)

Integrated nested vector interrupt controller, capable of handling up to 32 maskable interrupt channels (excluding 16 Core interrupt lines) and 4 priority levels.

- Tightly coupled NVIC achieves low-latency interrupt response processing
- Interrupt vector entry addresses directly enter the core
- Tightly coupled NVIC interface
- Allows early processing of interrupts
- Handles late-arriving higher priority interrupts
- Supports interrupt tail-chaining feature
- Automatically saves processor state
- Automatically restores on interrupt return, with no additional instruction overhead

External Interrupt/Event Controller (EXTI)

The external interrupt/event controller includes 32 edge detectors for generating interrupt/event requests. Each interrupt line can independently configure its trigger event (rising edge or falling edge or both edges) and can be masked independently; a pending register maintains the status of all interrupt requests. EXTI can detect pulses narrower than the internal APB2 clock cycle.

2.1.10 ADC (Analog/Digital Converter)

The 12-bit ADC has up to 10 external and two internal (temperature sensor, voltage reference measurement) channels and performs conversions in single trigger or scan mode. In scan mode, automatic conversions are performed on a set of selected analog inputs.

The ADC can be serviced by the DMA controller.

Supports analog watchdog feature. An interrupt is generated when the conversion voltage exceeds the programmed threshold.

2.1.11 COMP (Comparator)

Supports up to two fast rail-to-rail low-power comparators with programmable features of reference voltage (internal or external), hysteresis, and speed (low speed when in low power) and with selectable output polarity.

The reference voltage can be one of the following voltages:

- External IO
- Internal reference voltage or (1~13)/16 voltage divider

All comparators can wake up from Stop Mode, generate brake events, or send interrupts to the TIM module.

2.1.12 OPA (Operational Amplifier)

Supports up to three basic op-amp modules, which can implement basic signal amplification and signal operation functions with a few external components.

Features include:

- Gain-bandwidths supports 17MHz
- Supports rail-to-rail input/output
- The op-amp output can be connected to the internal comparator
- The op-amp output can be connected to the ADC channel
- Can be used as a comparator with external circuits

2.1.13 DIVSQRT (Division, Square Root Module)

Supports one 32bit/16bit hardware division module, which has the following features:

- Supports division of unsigned or signed numbers.
- Has overflow flag indicator.
- The dividend and quotient have a bit width of 32 bits, and the divisor and remainder have a bit width of 16 bits.
- Writing to the divisor register or the dividend register will both start the division operation.
- Completes operation in 8 HCLK clocks.
- Supports one 32bit hardware square root module, which has the following features:
- Writing to the radicand starts the square root operation.
- Completes operation in 8 HCLK clocks.

2.1.14 Temperature Sensor

The temperature sensor generates a voltage that changes linearly with temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel to convert the sensor's output to digital values.

2.1.15 Timers

Includes up to 1 advanced control timer, 6 general timers, and 2 basic timers.

The table below compares the features of advanced control timers, general timers, and basic timers:

Table 2 Comparison of Timer Features

Type	Timer	Counter Bit Width	Counting Method	Prescaler	DMA Request	Capture/Compare Channel	Complementary Output
Advanced Timer	TIM1	16bit	up / down / updown	Any integer between 1 and 65536	YES	4	3
Universal Timer	TIM2	32bit	up / down / updown		YES	4	-
	TIM3	16bit	up / down / updown		YES	4	-
	TIM14	16bit	up		NO	1	-
	TIM15	16bit	up		YES	1	1
	TIM16	16bit	up		YES	1	1
	TIM17	16bit	up		YES	1	1
Basic Timer	TIM6	16bit	up		YES	0	-
	TIM7	16bit	up		YES	0	-

Advanced Control Timer (TIM1)

The Advanced Control Timer (TIM1) can be seen as a three-phase PWM generator allocated to 6 channels. It has complementary PWM output with dead zone insertion and can also be used as a full general-purpose timer. Four independent channels can be used for:

- Input capture
- Output comparison
- PWM generation (edge or center-aligned mode)
- One-pulse output

When configured as a 16-bit standard timer, it has the same functionality as the general-purpose timer. When set as a 16-bit PWM generator, it has full modulation capability (0~100%). In debug mode, the counter can be frozen, and the PWM output is disabled.

Many functions are the same as the standard TIM timer, and the internal structure is also similar. Therefore, the Advanced Control Timer can work in conjunction with the TIM timer through the timer link function, providing synchronization or event chaining functions.

General-purpose Timer (TIM2, TIM3, TIM14, TIM15, TIM16, TIM17)

There are 6 synchronizable standard timers (TIM2, TIM3, TIM14, TIM15, TIM16, TIM17) in this product series. Each timer has a 16-bit (TIM2 is 32-bit) auto-reload increment/decrement counter, a 16-bit prescaler, and 4 (or 2 or 1) independent channels. Each channel can be used for input capture, output comparison, PWM, and one-pulse mode output. They can also work with the

Advanced Control Timer through the timer link function to provide synchronization or event chaining functions. In debug mode, the counter can be frozen. Any general-purpose timer can be used to produce PWM output.

Each timer has an independent DMA request mechanism.

These timers can also handle the signals from incremental encoders and can process the digital output of 1 to 3 Hall sensors.

Basic Timer TIM6 and TIM7

Used as a general 16-bit time base.

2.1.16 Watchdogs

Independent Watchdog

The independent watchdog is based on a 12-bit decrementing counter and an 8-bit prescaler, clocked by an independent 40kHz internal RC oscillator. As this RC oscillator is independent of the main clock, it can operate in stop and standby modes. It can be used as a watchdog to reset the entire system in case of problems or as a free-running timer to provide timeout management for applications. The option bytes can configure it to be software or hardware start watchdog. In debug mode, the counter can be frozen.

Window Watchdog

The window watchdog has a 7-bit decrementing counter and can be set to run freely. It can be used as a watchdog to reset the entire system in case of problems. It is driven by the main clock and has an early warning interrupt function. In debug mode, the counter can be frozen.

2.1.17 Systick Timer

This timer is specifically for real-time operating systems but can also be used as a standard countdown timer. Its features are:

- A 24-bit downward counter
- Auto-reload function
- Generates a maskable system interrupt when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

2.1.18 Real-Time Clock (RTC)

The RTC is an independent BCD timer/counter. Its main features are:

- Calendar with sub-second, seconds, minutes, hours (12 or 24 format), weekdays, dates, months, years, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap years), 30, and 31-day months.
- Programmable alarm wakeup capability from stop and standby modes.
- Periodic wakeup unit with programmable resolution and period.
- Real-time correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with the main clock.
- Digital calibration circuit with 1ppm resolution to compensate for the inaccuracy of the quartz crystal.
- Two tamper detection pins with a programmable filter. The MCU can be awakened from stop and standby modes when a tampering event is detected.
- Timestamp function, which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin or by a tampering event. The MCU can be awakened from stop and standby modes by timestamp event detection.
- Reference clock detection: A more accurate second source clock (50 or 60 Hz) can be used to enhance the calendar.
- RTC clock sources include:
- 32.768 kHz external crystal
- Oscillator or resonator
- Internal low-power RC oscillator (typical frequency of 40 kHz)
- High-speed external clock divided by 32

2.1.19 I2C

Up to two I2C interfaces (I2C1 and I2C2) can work in multi-master or slave modes. Both can support standard mode (up to 100Kbit/s) or fast mode (up to 400Kbit/s). I2C1 also supports Fast Mode Plus (up to 1Mbit/s) with a 20ma output driver. Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one configurable mask). They also include programmable analog and digital noise filters.

Table 3 I2C digital filtering and analog filtering

	Analog Filtering	Digital Filtering
Suppression of Spike Pulse Width	≥50 ns	Programmable width of 1-15 I2C clocks
Advantages	Available in stop mode	1. Enhanced filtering capability. Standard requirement. 2. Stable length.
Disadvantages	Varies with temperature, voltage, and process	-

In addition, I2C1 also provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP function, host notification protocol, hardware CRC (PEC) generation/verification, timeout validation, and ALERT protocol management.

The I2C interface can be serviced by the DMA controller.

For the differences between I2C1 and I2C2, please refer to the table below.

Table 4 I2C Features

I2C Features	I2C1	I2C2
7-bit Addressing Mode	X	X
10-bit Addressing Mode	X	X
Standard Mode (up to 100 kbit/s)	X	X
Fast Mode (up to 400 kbit/s)	X	X
Fast Mode Plus (up to 1 Mbit/s), 20mA output drive capability	X	X
Independent Clock	X	-
SMBUS	X	-
Wakeup from stop mode	X	-

2.1.20 USART

Up to 6 universal synchronous/asynchronous receivers/transmitters. All USART interfaces can be serviced by the DMA controller.

2.1.21 SPI

A maximum of two SPIs can communicate in both full-duplex and half-duplex communication modes, in slave and master modes. A 3-bit prescaler provides 8 master mode frequencies, with frame sizes configurable from 4 bits to 16 bits.

2.1.22 Serial Wire Debug Port (SW-DP)

Provides a serial debug port, allowing serial debugging tools to connect with the MCU.

3 Pin Definitions

TSSOP20 package

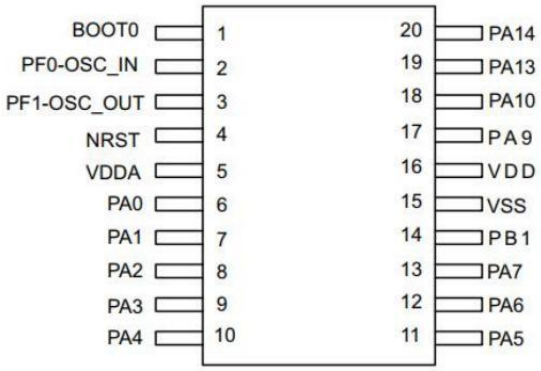


Figure 3: TSSOP20 package

LQFP32 package

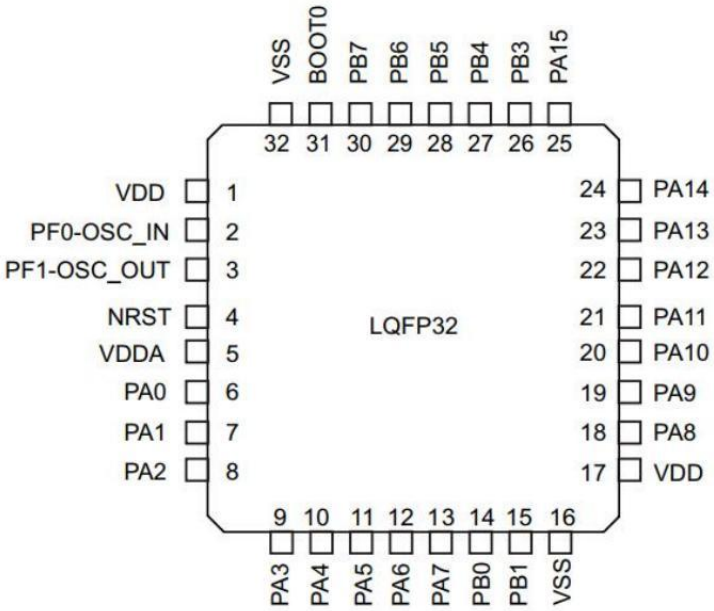


Figure 4: LQFP32 package

QFN32 package

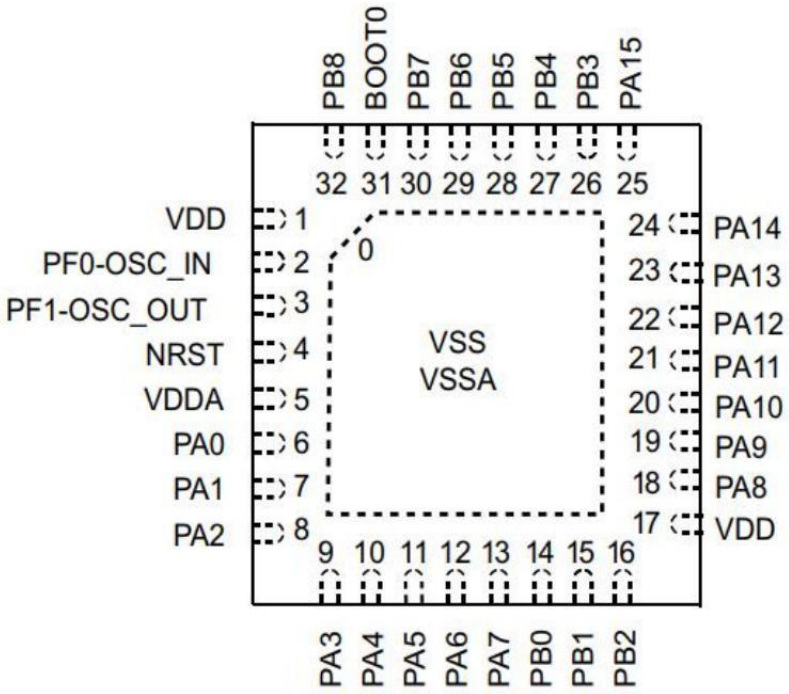


Figure 5: QFN32 package

LQFP48 package

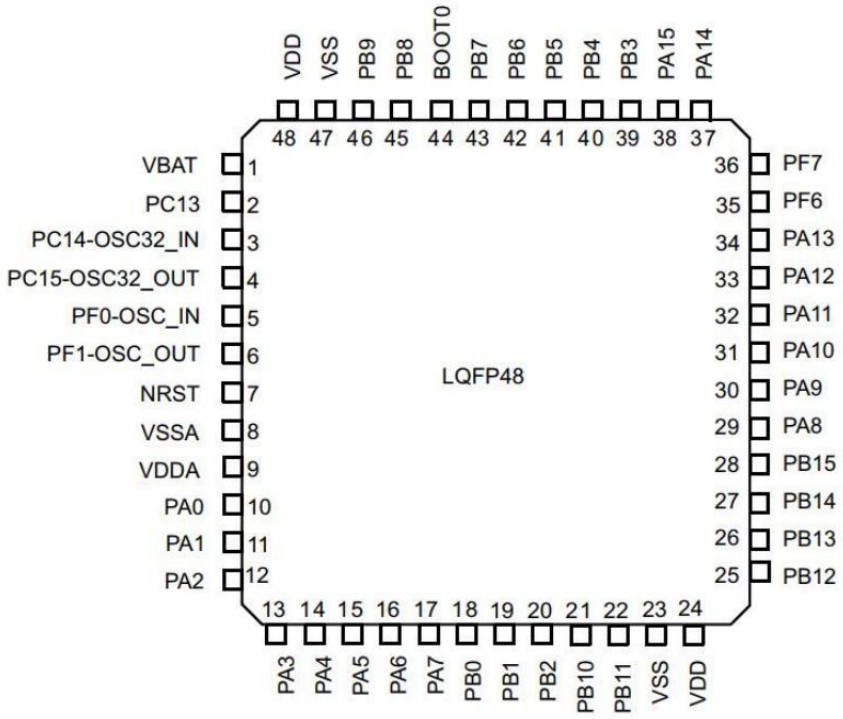


Figure 6: LQFP48 package

Pin definitions

Table 5: GPIOA_AFR configuration table

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PA0	-	USART1_CTS(1) USART2_CTS(2)	TIM2_CH1_ETR	-	USART4_TX	TIM2_CH4	TIM3_CH4	COMP1_OUT	-
PA1	EVENTOUT	USART1_RTS(1) USART2_RTS(2)	TIM2_CH2	-	USART4_RX	TIM15_CH1N	-	COMP2_OUT	-
PA2	TIM15_CH1	USART1_TX(1) USART2_TX(2)	TIM2_CH3	-	-	-	-	COMP2_OUT	-
PA3	TIM15_CH2	USART1_RX(1) USART2_RX(2)	TIM2_CH4	-	-	-	-	-	-
PA4	SPI1_NSS	USART1_CK(1) USART2_CK(2)	-	-	TIM14_CH1	USART6_TX	-	-	-
PA5	SPI1_SCK	-	TIM2_CH1_ETR	-	-	USART6_RX	-	-	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	USART3_CTS	TIM16_CH1	EVENTOUT	COMP1_OUT	-

PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT	-
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	-	-	TIM1_BKIN	TIM3_CH1	SPI2_MOSI
PA9	TIM15_BKIN	USART1_TX	TIM1_CH2	-	I2C1_SCL	MCO	-	TIM3_CH2	SPI2_NSS
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	-	I2C1_SDA	-	-	TIM3_CH3	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	-	USART2_TX	I2C2_SCL	TIM1_CH1N	COMP1_OUT	SPI2_SCK
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	-	USART2_RX	I2C2_SDA	TIM1_CH2N	COMP2_OUT	SPI2_MISO
PA13	SWDIO	IR_OUT	-	-	-	-	-	SPI2_MOSI	USART3_TX
PA14	SWCLK	USART1_TX(1) USART2_TX(2)	-	-	-	-	-	SPI2_NSS	USART3_RX
PA15	SPI1_NSS	USART1_RX(1) USART2_RX(2)	TIM2_CH1_ETR	EVENTOUT	USART4_RTS	-	-	TIM1_CH3N	TIM1_BKIN

1, Only present in the x8 model.

2, Only present in the xB and xC models.

Table 6: GPIOB_AFR configuration table

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-	USART3_CK	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	USART3_RTS	-	-	-	-
PB2	-	-	-	-	USART4_CK	-	-	-	-
PB3	SPI1_SCK	EVENTOUT	TIM2_CH2	-	USART5_TX	-	TIM2_CH1_ETR	TIM1_CH2N	TIM3_CH3
PB4	SPI1_MISO	TIM3_CH1	EVENTOUT	-	USART5_RX	TIM17_BKIN	TIM2_CH2	TIM1_CH1N	I2C2_SCL
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	USART5_CK	-	TIM2_CH3	TIM1_CH3	I2C2_SDA
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	-	-	-	-	TIM1_CH2	SPI2_SCK
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	-	USART4_CTS	-	-	TIM1_CH1	SPI2_MISO
PB8	-	I2C1_SCL	TIM16_CH1	-	-	-	-	COMP1_OUT	USART2_TX
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT	-	SPI2_NSS	-	COMP2_OUT	USART2_RX
PB10	-	I2C1_SCL(1) I2C2_SCL(2)	TIM2_CH3	-	USART3_TX	SPI2_SCK	-	-	-
PB11	EVENTOUT	I2C1_SDA(1) I2C2_SDA(2)	TIM2_CH4	-	USART3_RX	-	-	-	-
PB12	SPI1_NSS(1) SPI2_NSS(2)	EVENTOUT	TIM1_BKIN	-	USART3_CK	TIM15_BKIN	-	-	-
PB13	SPI1_SCK(1) SPI2_SCK(2)	-	TIM1_CH1N	-	USART3_CTS	I2C2_SCL	-	-	-
PB14	SPI1_MISO(1) SPI2_MISO(2)	TIM15_CH1	TIM1_CH2N	-	USART3_RTS	I2C2_SDA	-	-	-

PB15	SPI1_MOSI(1) SPI2_MOSI(2)	TIM15_CH2	TIM1_CH3N	TIM15_CH1N	-	-	-	-	-

1, Only present in the x8 model.

2, Only present in the xB and xC models.

Table 7 GPI0F_AFR

Pin name	AF0	AF1	AF7	AF8
PF0	-	I2C1_SDA	TIM1_BKIN	SPI2_MOSI
PF1	-	I2C1_SCL	TIM14_CH1	SPI2_NSS
PF6	I2C1_SCL(1), I2C2_SCL(2)	-		SPI2_MOSI
PF7	I2C1_SDA(1), I2C2_SDA(2)	-		SPI2_NSS

1, Only present in the x8 model.

2, Only present in the xB and xC models.

ADC PIN

Pin **name**	ADC **Channel**
PA0	ADC1_CH0
PA1	ADC1_CH1
PA2	ADC1_CH2
PA3	ADC1_CH3
PA4	ADC1_CH4
PA5	ADC1_CH5
PA6	ADC1_CH6
PA7	ADC1_CH7
PB0	ADC1_CH8
PB1	ADC1_CH9

4. Electrical Characteristics

Test Conditions

Unless otherwise specified, all voltages are referenced to VSS.

4.1.1 Maximum and Minimum Values

Unless otherwise specified, the maximum and minimum values are guaranteed under the worst conditions of ambient temperature, supply voltage, and clock frequency, determined by testing 100% of the products under TA = 25℃ and TA = TA max (as given by the selected temperature range). Notes under tables may indicate that some data is derived from calculations, design simulations, and/or process characteristics and is not tested on the production line. Minimum and maximum values are derived from sample tests and are taken as the average value plus or minus three times the standard deviation (average ±3Σ).

4.1.2 Typical Values

Unless otherwise specified, typical values are based on a testing environment of TA = 25℃ and VDD = 3.3V. This data is for design guidance only and has not been experimentally validated.

4.1.3 Typical Curves

Unless otherwise specified, all typical curves are for design guidance only and have not been experimentally validated.

4.1.4 Load Capacitance

The load conditions for measuring pin parameters are shown below:

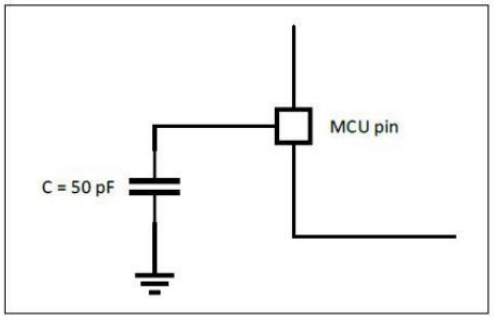


Figure 7: Pin Load Conditions

4.1.5 Pin Input Voltage

The method for measuring pin input voltage is shown below:

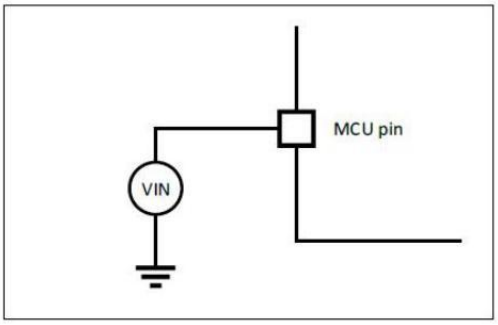


Figure 8: Pin Input Voltage Measurement

4.1.6 Power Supply Scheme

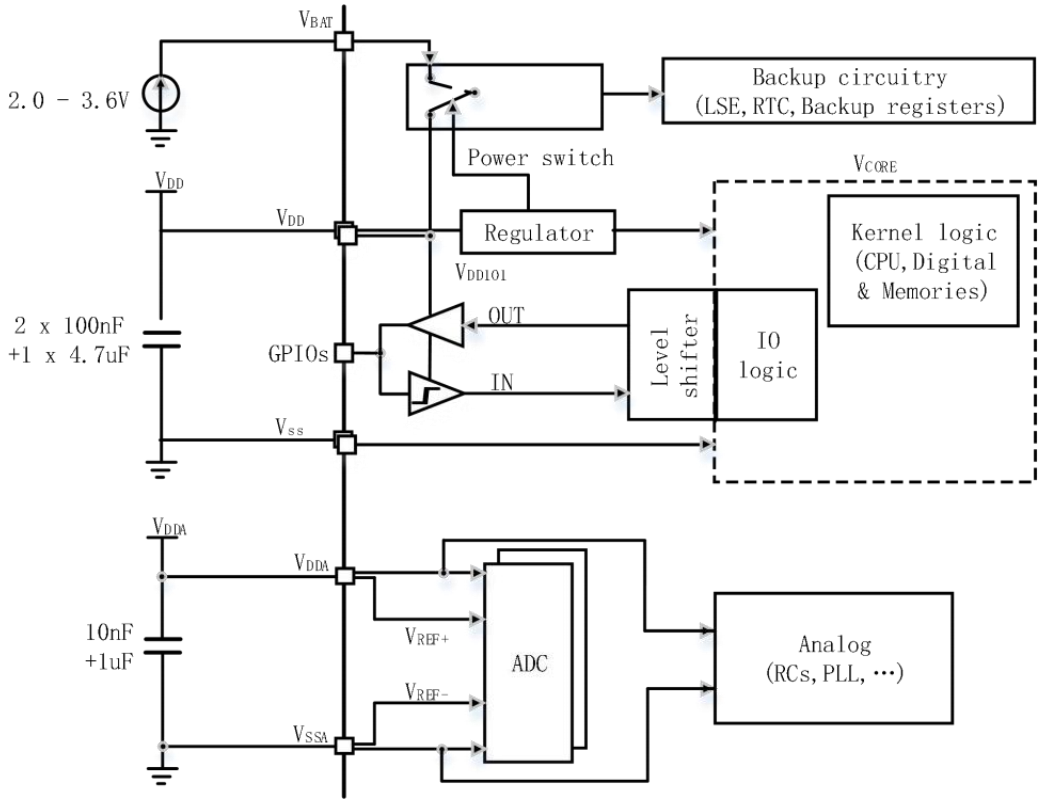


Figure 9: Power Supply Scheme

4.1.7 Current Consumption Measurement

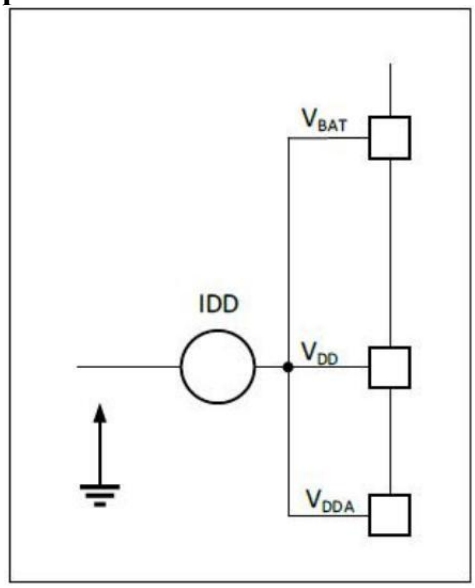


Figure 10: Current Consumption Measurement Scheme

Absolute Maximum Ratings

4.1.8 Electrical Performance Parameters

The limit values listed below can cause permanent damage to the chip. The chip may not operate properly under these extreme conditions. Operating at the maximum rated conditions for extended periods may affect the reliability of the chip.

Table 8: General Operating Conditions

Symbol	Description	Min	Max	Unit
VDD - VSS	External main supply voltage (including VDDA and VDD)(1)	-0.3	4	V
VIN	Input voltage on 5V tolerant pins	Vss-0.3	6	
	Input voltage on other pins(2)	Vss-0.3	4.0	
ΔVDDx	Voltage difference between different supply pins	—	50	mV
VSSx-VSS	Voltage difference between different ground pins	—	50	

1: All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to an external supply system

within the allowable range.

Table 9: Current Characteristics

Symbol	Description	Max(1)	Unit
IVDD	Total current passing through the VDD/VDDA power line (supply current) (1)	150	mA
IVSS	Total current through the VSS ground wire (outgoing current) (1)	150	
IIO	Sink current on any I/O and control pins	25	
	Source current on any I/O and control pins	-25	

1: All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to an external supply system within the allowable range.

Table 10: Temperature Characteristics

Symbol	Description	Value	Unit
TSTG	Storage temperature range	-40 ~ +105	℃
TJ	Maximum junction temperature	125	℃

4.1.9 Power-up and Power-down Operating Conditions

The parameters given in the table below are based on the general operating conditions and tested at the listed ambient temperatures.

Table 11: Power-up and Power-down Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
tVDD	VDD Rising Speed	—	0	∞	us/V
	VDD Falling Speed		20	∞	

4.1.10 Embedded Reset and Power Control Module Characteristics

The parameters given in the table below are based on the general operating conditions and tested under the VDD supply voltage.

Table 12: Embedded Reset and Power Control Module Characteristics

Symbol	Parameter	Condition	Min	Typical	Max	Unit
VPVD	Electrical Level Selection of Programmable Voltage Detector	PLS[2:0]=000 (rising edge)	—	2.21	—	V
		PLS[2:0]=000 (falling edge)	—	2.14	—	V
		PLS[2:0]=001 (rising edge)	—	2.31	—	V
		PLS[2:0]=001 (falling edge)	—	2.24	—	V
		PLS[2:0]=010 (rising edge)	—	2.41	—	V
		PLS[2:0]=010 (falling edge)	—	2.34	—	V
		PLS[2:0]=011 (rising edge)	—	2.51	—	V
		PLS[2:0]=011 (falling edge)	—	2.44	—	V
		PLS[2:0]=100 (rising edge)	—	2.61	—	V
		PLS[2:0]=100 (falling edge)	—	2.54	—	V
		PLS[2:0]=101 (rising edge)	—	2.71	—	V
		PLS[2:0]=101 (falling edge)	—	2.64	—	V
		PLS[2:0]=110 (rising edge)	—	2.81	—	V
		PLS[2:0]=110 (falling edge)	—	2.74	—	V
		PLS[2:0]=111 (rising edge)	—	2.91	—	V
		PLS[2:0]=111 (falling edge)	—	2.84	—	V
VPVDhyst(1)	PVD Delay	—	—	70	—	mV
VPOR/PDR	Power on/off Reset Threshold	falling edge	—	1.72	—	V
		rising edge	—	1.76	—	V
VPDRhyst(1)	PDR Delay	—	—	40	—	mV
TRSTTEMPO (1)	Reset Duration	—	—	2	—	ms

Guaranteed by design, not tested in production.

4.1.11 Internal Reference Voltage

Parameters given in the table below are tested under the general operating condition listed VDD power supply voltage.

Table 13: Internal Reference Voltage

Symbol	Parameter	Condition	Min	Typical	Max	Unit
VREFINT	Internal Reference Voltage	-40℃ < TA < +105℃	1.2	1.23	1.25	V
TS_vrefint(1)	ADC sampling time when reading the internal reference voltage	—	-	5.1	17.5	μs

1, The shortest sampling time is obtained through multiple loops in the application.

2, Guaranteed by design, not tested in production.

4.1.12 Power Supply Current Characteristics

The current consumption is a composite indicator of various parameters and factors, including operating voltage, ambient temperature, I/O pin load, software configuration of the product, operating frequency, flip rate of the I/O pin, position of the program in memory, and executed code, etc.

For a detailed explanation of the measurement method of current consumption, refer to the current consumption test amount in the test conditions section.

Conditions for measuring current consumption of the microcontroller:

. All I/O pins are in analog input mode.
. All peripherals are turned off unless otherwise specified.
. When turning on peripherals: fPCLK1 = fHCLK/2, fPCLK2 = fHCLK.

Table 14: Current Consumption in Operating Mode

Symbol	Parameter	Condition	fHCLK	Typical Value(1)		Maximum Value(2)		Unit
				Enable All Peripherals	Close All Peripherals	Enable All Peripherals	Close All Peripherals	
			72MHz	10.6	6.6	11.6	7.4	
			48MHz	8.0	5.3	9.0	6.1	
			32MHz	6.3	4.4	7.1	5.2	
			24MHz	5.4	4.0	6.2	4.7	
			16MHz	4.5	3.5	5.3	4.2	mA
			8MHz	3.4	2.9	4.5	4.0	
		High Speed	64MHz	9.7	6.1	11.1	7.1	
			48MHz	8.0	5.3	9.2	6.2	
			32MHz	6.3	4.4	7.3	5.3	

		Internal RC Oscillator (HSI)	24MHz	5.4	4.0	6.3	4.6	
			16MHz	4.5	3.5	5.3	4.3	
			8MHz	3.4	2.9	4.6	4.0	

1,Typical values are tested at TA=25℃, VDD=3.3V.

2,Maximum values are tested at TA= 105℃, VDD=3.6V.

3,External clock is 8MHz; PLL is enabled when fHCLK>8MHz.

Table 15 :Current consumption in sleep mode, code running in Flash.

Symbol	Parameter	Condition	fHCLK	Typical Value(1)		Maximum Value(2)		Unit
				Enable All Peripherals	Close All Peripherals	Enable All Peripherals	Close All Peripherals	
IDD	Supply Current Under Sleep Mode	External Clock(3)	72MHz	8.9	4.3	9.8	5.1	mA
			48MHz	6.8	3.8	7.7	4.5	
			32MHz	5.4	3.4	6.3	4.1	
			24MHz	4.8	3.2	5.6	3.9	
			16MHz	4.1	3.0	4.8	3.7	
			8MHz	3.2	2.7	4.3	3.3	
		High Speed Internal RC Oscillator (HSI)	64MHz	8.2	4.1	9.4	5.0	
			48MHz	6.8	3.8	7.9	4.5	
			32MHz	5.4	3.4	6.4	4.1	
			24MHz	4.8	3.2	5.7	3.9	
			16MHz	4.1	3.0	4.9	3.7	
			8MHz	3.8	2.7	4.3	3.4	

1. Typical values are tested at TA=25℃ and VDD=3.3V.
2. Maximum values are tested at TA= 105℃ and VDD=3.6V.
3. External clock is 8MHz; PLL is enabled when fHCLK>8MHz.

Table 16: Typical and maximum current consumption in shutdown and standby modes.

Symbol	Parameter	Condition	Typical Value(1)	Maximum Value(2)	Unit
IDD	Supply Current Under Stop Mode	The regulator is in operating mode. Low-speed, high-speed internal RC Oscillator, and external high-speed Oscillator are turned off (no independent watchdog).	80	—	uA
		The regulator is in low-power mode. Low-speed, high-speed internal RC Oscillator, and external high-speed Oscillator are turned off (no independent watchdog).	15	—	
	Supply Current	The low-speed internal RC Oscillator, external low-speed Oscillator, RTC, and IWDG are	1.3	—	

	Under Standby Mode	turned off.			
		The low-speed internal RC Oscillator is turned on; the external low-speed Oscillator, RTC, and IWDG are turned off.	1.8	—	
		The external low-speed Oscillator is turned on; the low-speed internal RC Oscillator, RTC, and IWDG are turned off.	2.1	—	
		The external low-speed Oscillator and RTC are turned on; the low-speed internal RC Oscillator and IWDG are turned off.	2.6	—	
		The low-speed internal RC Oscillator and IWDG are turned on; the external low-speed Oscillator and RTC are turned off.	1.8	—	
IDD_VBAT	Supply Current in Backup Area	The external low-speed Oscillator and RTC are turned on.	1.5	—	
		The external low-speed Oscillator and RTC are turned off.	0.2	—	

1. Typical values are tested at TA=25℃ and VDD=3.3V.
2. Maximum values are tested at TA= 105℃ and VDD=3.6V.
3. The external clock is 8MHz, and PLL is enabled when fHCLK>8MHz.

4.1.13 External Clock Source Characteristics

An external high-speed clock produced using a crystal/ceramic resonator.

The high-speed external clock (HSE) can be generated using an oscillator comprised of a 4~32MHz crystal/ceramic resonator. The information provided in this section is based on the results obtained from an overall feature evaluation using the typical external components listed in the table below. In applications, the resonator and the load capacitance must be as close as possible to the oscillator's pins to minimize output distortion and stabilization time during startup. For detailed parameters of the crystal resonator (frequency, packaging, precision, etc.), please consult the respective manufacturer. (Translator's note: The crystal resonator mentioned here is what we commonly refer to as a passive crystal.)

Table 17: HSE 4~32MHz Oscillator Features

Symbol	Parameter	Condition		Minimum Value	Typical Value	Maximum Value	Unit
fOSC_IN	Oscillator Frequency	—		4	8	32	MHz
tSU(HSE)	Starting Time	VDD is stable	TA = -40℃	—	2	—	ms
			TA = 25 ℃	—	1.9	—	
			TA =	—	2.1	—	

			85 ℃				

1. The resonator's characteristic parameters are provided by the crystal/ceramic resonator manufacturer.
2. Derived from a comprehensive evaluation, not tested in production.
3. tSU(HSE) is the startup time, measured from the moment the software enables the HSE until a stable 8MHz oscillation is achieved. This value is measured on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

For CL1 and CL2, it is recommended to use high-quality ceramic capacitors designed for high-frequency applications (with typical values between) 5 pF and 25 pF. Choose a crystal or resonator that meets the requirements. Typically, CL1 and CL2 have the same parameters. Crystal manufacturers usually provide load capacitance parameters based on the serial combination of CL1 and CL2. When selecting CL1 and CL2, the capacitance of the PCB and MCU pins should be considered (you can roughly estimate the capacitance between the pins and the PCB board as 10 pF).

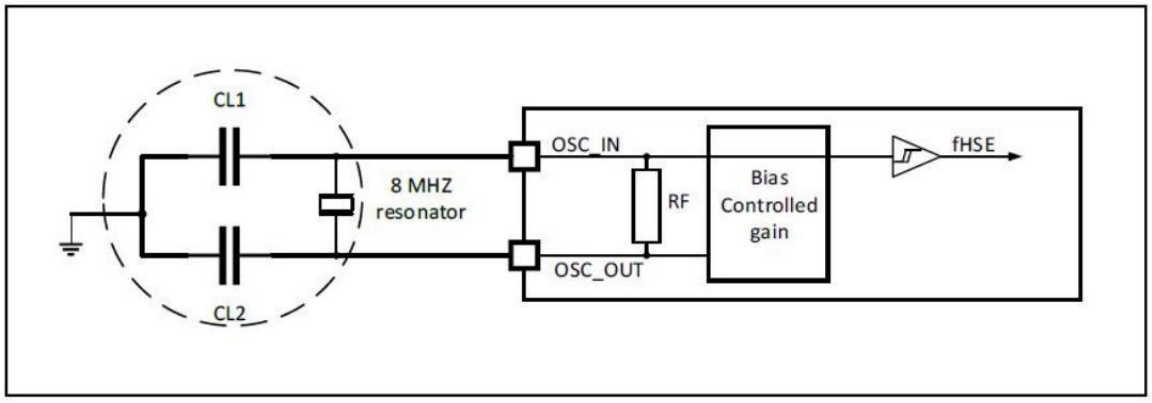


Figure 11: Typical application using an 8MHz crystal

An external low-speed clock produced using a crystal/ceramic resonator.

The low-speed external clock (LSE) can be generated using an oscillator comprised of a 32.768kHz crystal/ceramic resonator. The information provided in this section is based on results obtained from an overall feature evaluation. In applications, the resonator and load capacitance must be as close as possible to the oscillator's pins to minimize output distortion and stabilization time during startup. For detailed parameters about the crystal resonator (frequency, packaging, precision, etc.), please consult the respective manufacturer. (Translator's note: The crystal resonator mentioned here is what we commonly refer to as a passive crystal.)

Table 18: LSE Oscillator Features (fLSE=32.768kHz)

Symbol	Parameter	Condition		Minimum Value	Typical Value	Maximum Value	Unit
tSU(HSE)	Starting Time	VDD is stable	TA = -40℃	—	—	300	ms
			TA = 25 ℃	—	—	400	
			TA = 105 ℃	—	—	500	

1.Derived from a comprehensive evaluation, not tested in production.

For CL1 and CL2, it is recommended to use high-quality ceramic capacitors ranging between 5 pF and 15 pF, and select a crystal or resonator that meets the requirements. Typically, CL1 and CL2 have the same parameters. Crystal manufacturers usually specify the load capacitance based on the serial combination of CL1 and CL2.

The load capacitance CL is calculated by the following formula: CL = CL1 x CL2 / (CL1 + CL2) + Cstray, where Cstray represents the capacitance of the pin and PCB board or related PCB capacitance. Its typical value ranges between 2 pF and 7 pF.

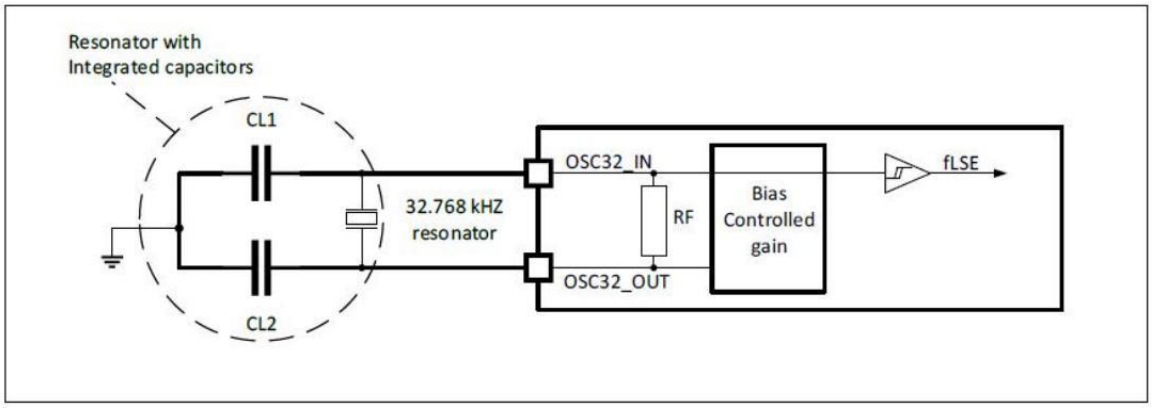


Figure 12: Typical application using a 32.768KHz crystal

4.1.14 Internal Clock Source Characteristics

The characteristic parameters given in the table below were measured under general working conditions, consistent with environmental temperature and power supply voltage.

High-Speed Internal (HSI) RC Oscillator

Table 19: HSI Oscillator Features

Symbol	Parameter	Condition	Minimum Value	Typical Value	Maximum Value	Unit
fHSI	Frequency	—	—	8	—	MHz
ACCHSI	HIS Oscillator precision	TA = 25℃(LSE no Calibration)	-1	—	1	%
		TA = -40~70℃(LSE No Calibration)	—	+-1.5	—	%
		TA = 70~105℃(LSE No Calibration)	—	+-3	—	%
		TA = -40~105℃(LSE Calibration)	-1	—	1	%
tSU(HSI)	HIS Oscillator Starting Time	—	—	—	2	us

1, VDD = 3.3V, TA = -40~105℃, unless otherwise specified.

High-Speed Internal 14MHz (HSI14) RC Oscillator (Dedicated for ADC)

Table 20: HSI14 Oscillator Features

Symbol	Parameter	Condition	Minimum Value	Typical Value	Maximum Value	Unit
fHSI14	Frequency	—	—	14	—	MHz
ACCHSI14	HSI14 Oscillator Precision	TA = -40~105℃	—	+-3	—	%
tSU(HSI14)	HSI14 Oscillator Starting Time	—	—	—	2	us
IDD(HSI14)	HSI14 Oscillator Power Consumption	—	—	100	—	uA

Low-Speed Internal (LSI) RC Oscillator

Table 21: LSI Oscillator Features

Symbol	Parameter	Condition	Minimum Value	Typical Value	Maximum Value	Unit
fLSI(2)	Frequency	—	—	40	—	kHz
tSU(LSI)(3)	LSI Oscillator Starting Time	—	—	34.3	—	us
IDD(LSI)(3)	LSI Oscillator Power Consumption	—	—	0.5	—	uA

1 VDD = 3.3V, TA = -40~105℃, unless otherwise specified.
2 Derived from an overall assessment, not tested in production.
3 Guaranteed by design, not tested in production.

4.1.15 Wake-up Time from Low-Power Modes

The wake-up times listed in the table below are measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used upon wake-up depends on the current operating mode:

. Stop or Standby mode: The clock source is the RC oscillator.
. Sleep mode: The clock source is the one used when entering sleep mode.

All times are measured under general working conditions with the given environmental temperature and supply voltage.

Table 22: Wake-up Times from Low-Power Modes

Symbol	Parameter	Typical Value	Unit
tWUSLEEP(1)	Wake-up from Sleep mode	10	CPU clock cycle
tWUSTOP(1)	Wake-up from Stop mode (regulator in low-	20	μs

	power)		
tWUSTDBY(1)	Wake-up from Standby mode	230	μs

1.The wake-up time measurement starts from the wake-up event until the first instruction of the user program is read.

4.1.16 PLL Characteristics

The parameters listed in the following table are measured under general operating conditions of ambient temperature and power supply voltage.

Table 23: PLL Characteristics

Symbol	Parameter	Value			Unit
		Minimum Value	Typical Value	Maximum Value(1)	
fPLL_IN	PLL Input Clock(2)	1	8	32	MHz
	PLL Input Clock Duty Cycle	40	—	60	%
fPLL_OUT	PLL Frequency Multiplied Output Clock	4	—	72	MHz
tLOCK	PLL Phase Lock Time	—	50	60	us

1.Derived from comprehensive evaluation, not tested in production.

2. It's important to use the correct multiplication factor so that the fPLL_OUT is within the allowable range based on the PLL input clock frequency.

4.1.17 Memory Characteristics

Flash Memory

Unless specified otherwise, all characteristic parameters are obtained at TA = -40~85℃.

Table 24: Flash Memory Characteristics

Symbol	Parameter	Condition	Typical Value
tPROG	16-bit programming time	—	65
tERASE	Page erase time	—	10
tME	Full chip erase time	—	10

Table 25: Flash Memory Lifetime and Data Retention Period

Symbol	Parameter	Condition	Min Value(1)	Typical Value	Max Value	Unit
NEND	Lifespan (Note: Erase/Write Cycles)	TA = -40~105℃	300	—	—	Thousand times
tRET	Data Retention Duration	TA = 125℃	20	—	—	Years

1.Determined by a comprehensive assessment, not tested during production.

4.1.18 Absolute Maximum Ratings (Electrical Sensitivity)

Electrostatic Discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse after a one-second interval) is applied to all pins of all samples. The size of the sample is related to the number of power pins on the chip (3 pieces x (n+1) power pins). This test complies with the JEDEC EIA/JESD22-A114 standard.

Table 26: ESD Absolute Maximum Ratings.

Symbol	Parameter	Condition	Maximum Value(1)	Unit
VESD(HBM)	Electrostatic Discharge Voltage (Human Body Model)	T A = +25 °C, in accordance with JEDEC EIA/JESD22-A114	5000	V

1, Determined through comprehensive evaluation and not tested during production.

4.1.19 I/O Port Characteristics

General Input/Output Characteristics

Unless otherwise specified, the parameters listed in the table below are measured under standard operating conditions. All I/O ports are compatible with CMOS and TTL.

Table 27: I/O Static Characteristics

Symbol	Parameter	Condition	Minimum Value	Typical Value	Maximum Value	Unit
VIL	Input low-level voltage	—		—	1.5	V
VIH	Standard I/O pin, input high-level voltage		1.8	—	—	
	FT I/O pin, input high-level voltage		1.8	—	—	
Vhys	Standard I/O pin Schmitt trigger voltage hysteresis	—	—	0.3	—	V
	5V tolerant I/O pin Schmitt trigger voltage hysteresis		—	0.3	—	V
Ilkg	Input leakage current	VSS ≤ VIN ≤ VDD Standard I/O Port	—	—	<0.1	uA

		VIN = 5V， 5V Tolerate Port	—	—	<0.1	
RPU	Weak pull-up equivalent resistance	VIN = VSS	—	37	—	kΩ
RPD	Weak pull-down equivalent resistance	VIN = VDD	—	37	—	kΩ

Output Voltage

Unless otherwise specified, the parameters listed in the following table are measured under general operating conditions using the ambient temperature and VDD power supply voltage. All I/O ports are compatible with CMOS and TTL.

Table 28: Output Voltage Characteristics.

Symbol	Parameter	Conditions	Min	Max	Unit
VOL	Output Low Level	Standard I/O port, I_{IO} = -17mA, VDD=3.3V	—	0.4	V
VOH	Output High Level	Standard I/O port, I_{IO} = 14mA, VDD=3.3V	2.9	—	
VOL	Output Low Level	5V Tolerant port, I_{IO} = -17mA, VDD=3.3V	—	0.4	
VOH	Output High Level	5V Tolerant port, I_{IO} = 14mA, VDD=3.3V	2.9	—	
VOL	Output Low Level	Backup domain I/O port(1), I_{IO} = -17mA, VDD=3.3V	—	0.4	
VOH	Output High Level	Backup domain I/O port(1), I_{IO} =6mA VDD-3.3V	2.9	—	

1, The backup domain I/O ports refer to PC13~PC15.

4.1.20 NRST Pin Characteristics

The NRST pin input is driven by CMOS technology, and it is connected to an inseparable pull-up resistor.

Unless otherwise specified, the parameters listed in the table below are measured under general working conditions of ambient temperature and supply voltage.

Table 29: NRST Pin Characteristics

Symbol	Parameter	Condition	Min	Typical	Max	Unit
VIL(NRST)(1)	NRST Input Low-Level Voltage	—	—	1.5	—	V
VIH(NRST)(1)	NRST Input High-Level Voltage	—	—	1.8	—	
Vhys(NRST)	NRST Schmitt Trigger Voltage Hysteresis	—	—	300	—	mV

RPU	Weak Pull-up Equivalent Resistance	VIN=VSS	—	37	—	kΩ
VF(NRST)(1)	NRST Input Filtered Pulse	—	—	120	—	ns
VNF(NRST)(1)	NRST Input Non-filtered Pulse	—	25	—	—	ns

1. Guaranteed by design, not tested in production.

Recommended Protection for NRST Pin

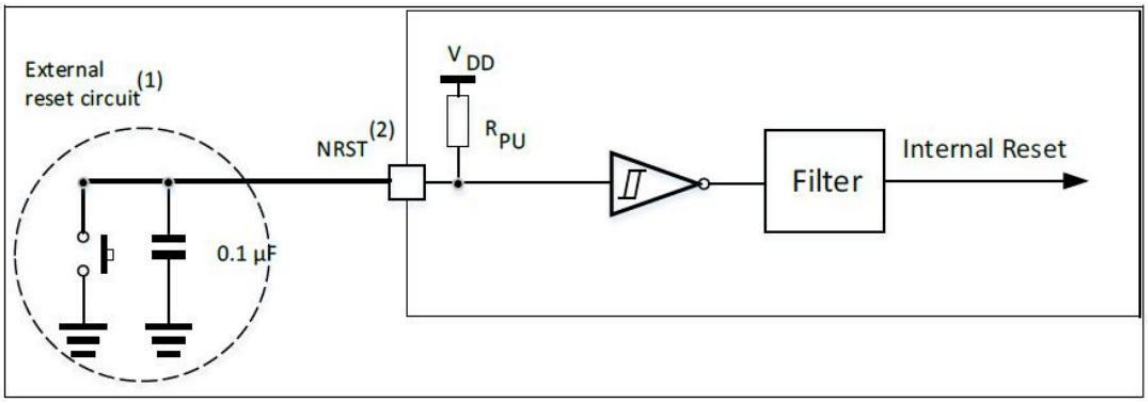


Figure 13: Recommended Protection for NRST Pin

1. The reset network is designed to prevent parasitic resets.

2. Users must ensure that the voltage on the NRST pin remains below the maximum VIL(NRST) value; otherwise, the MCU will not reset.

4.1.21 12-bit ADC Characteristics

Unless otherwise stated, the parameters in the following table are measured under standard operating conditions of ambient temperature, fPCLK2 frequency, andVDDA supply voltage.

Note: It is recommended to calibrate once each time the power is turned on.

Table 30: ADC Characteristics.

Symbol	Parameter	Condition	Minimum Value	Typical Value	Maximum Value	Unit
VDDA	Supply Voltage	—	1.8	3.3	3.6	V
VREF+	Positive Reference	—	2.4	—	VDDA	V

	Voltage					
fADC	ADC Clock Frequency	—	0.6	—	14	MHz
fS(2)	Sampling Rate	—	0.05	—	1	MHz
fTRIG(2)	External Trigger Frequency	fADC = 14MHz	—	—	823	kHz
VAIN	Conversion Voltage Range (3)	—	0	—	VREF+	V
RAIN(2)	External Input Impedance	—	—	—	50	kΩ
RADC(2)	Sampling Switch Resistance	—	—	—	1	kΩ
tCAL(2)	Calibration Time	fADC = 14MHz	5.9			us
			83			1/fADC
tlatr(2)	Trigger Conversion Delay	fADC = fPCLK/2 = 14 MHz	0.196			us
		fADC = fPCLK/2	5.5			1/fPCLK
		fADC = fPCLK/4 = 12 MHz	0.219			us
		fADC = fPCLK/4	10.5			1/fPCLK
		fADC = fHSI14 = 14 MHz	0.188	—	0.259	us
tS(2)	Sampling Time	fADC = 14MHz	0.107	—	17.1	us
		—	1.5	—	239.5	1/fADC
tSTAB(2)	Stabilization Time	—	0	0	1	us
tCONV(2)	Total Conversion Time (including sampling)	fADC = 14MHz	1	—	18	us
			14 to 252 （ts+ 12.5 used for successive approximation）			1/fAD

				C

1. Guaranteed by comprehensive evaluation, not tested during production.
2. Guaranteed by design, not tested during production.
3. Depending on the package, VREF+ can be internally connected to VDDA, and VREF- can be internally connected to VSSA.
4. For external triggering, a delay of 1/fPCLK2 must be added to the listed delays.

Table 31: Maximum RAIN when fADC = 14MHz.

TS(Cycle)	tS(us)	Maximum RAIN(kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	-
239.5	17.11	-

1. Guaranteed by design, not tested during production.

4.1.22 Temperature Sensor Characteristics

Table 32: Temperature Sensor Characteristics.

Symbol	Parameter	Min	Typical	Max	Unit
Avg_Slope(1)	Average Slope	—	4.3	—	mV/ºC
V25(1)	Voltage at 30ºC (±5ºC)	—	1.43	—	V
tSTART(2)	Startup Time	—	—	10	µs
TS_temp(2)(3)	ADC Sample Time when reading temperature	—	—	17.1	µs

1. Ensured by comprehensive assessment, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined by the application through multiple loops.

The temperature is calculated using the following formula:

Temperature (ºC) = {(V30 – VSENSE) / Avg_Slope} + 30

Where V30 = VSENSE value at 30 °C

Avg_Slope = Average slope of the temperature vs VSENSE curve (in mV/°C)

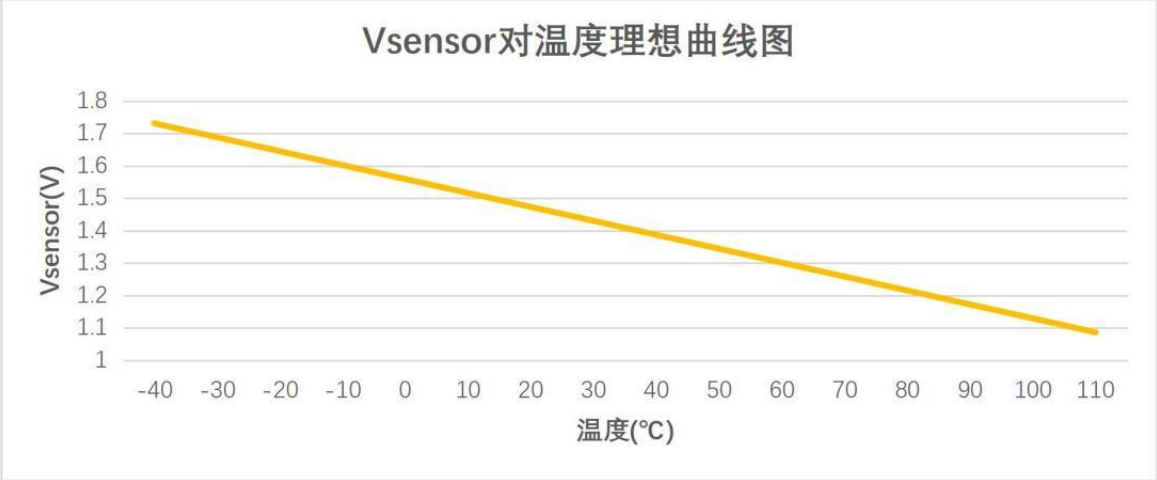


Figure 14: Ideal VSENSE vs. Temperature Curve

4.1.23 COMP Electrical Characteristics

Table 33: COMP Characteristics

Symbol	Parameter	Condition	Min	Typical	Max	Unit
VDDA	Voltage Range	—	1.8	—	3.6	V
VIN	Comparator Input Voltage Range	—	0	—	VDDA	V
tSTART	Comparator Starting Time	—	—	—	60	us
tD	Input 1KHz square wave = 0.1~0.3V, Reference voltage = 0.2V	Ultra-Low-Speed Mode	—	0.47	—	us
		Low-Speed Mode	—	0.25	—	
		Medium-Speed Mode	—	0.14	—	
		High-Speed Mode VDDA >= 2.7V	—	47	—	ns
		High-Speed Mode VDDA < 2.7V	—	45	—	
	Input 1KHz square wave = 1.1~1.3V, Reference voltage = 1.2V	Ultra-Low-Speed Mode	—	0.57	—	us
		Low-Speed Mode	—	0.29	—	
		Medium-Speed Mode	—	0.15	—	
		High-Speed Mode VDDA >= 2.7V	—	50	—	ns

		High-Speed Mode VDDA < 2.7V	—	44	—	
	Input 1KHz square wave = 0~2.4V, Reference voltage = 2.3V	Ultra-Low-Speed Mode	—	0.47	—	us
		Low-Speed Mode	—	0.25	—	
		Medium-Speed Mode	—	0.22	—	
		High-Speed Mode VDDA >= 2.7V	—	96	—	ns
		High-Speed Mode VDDA < 2.7V	—	93	—	
Voffset	Offset Error	—	—	+-5	—	mV
IDD(COMP)	Comparator Power Consumption	Ultra-Low-Speed Mode	—	1.2	—	uA
		Low-Speed Mode	—	2.4	—	
		Medium-Speed Mode	—	4.8	—	
		High-Speed Mode	—	19.2	—	
Vhys	Comparator Hysteresis	No Hysteresis Configuration (COMPxHYST[1:0] = 00)	—	0	—	mV
		Low Hysteresis Configuration and High-Speed Mode (COMPxHYST[1:0] = 01)	—	7	—	
		Low Hysteresis Configuration and Non-High-Speed Mode (COMPxHYST[1:0] = 01)	—	5	—	
		Medium Hysteresis Configuration and High-Speed Mode (COMPxHYST[1:0] = 10)	—	15	—	
		Medium Hysteresis	—	11	—	

		Configuration and Non-High-Speed Mode (COMPxHYST[1:0] = 10)				
		High Hysteresis Configuration and High-Speed Mode (COMPxHYST[1:0] = 10)	—	32	—	
		High Hysteresis Configuration and Non-High-Speed Mode (COMPxHYST[1:0] = 10)	—	24	—	

4.1.24 OPA Electrical Characteristics

Table 34:OPA Characteristics

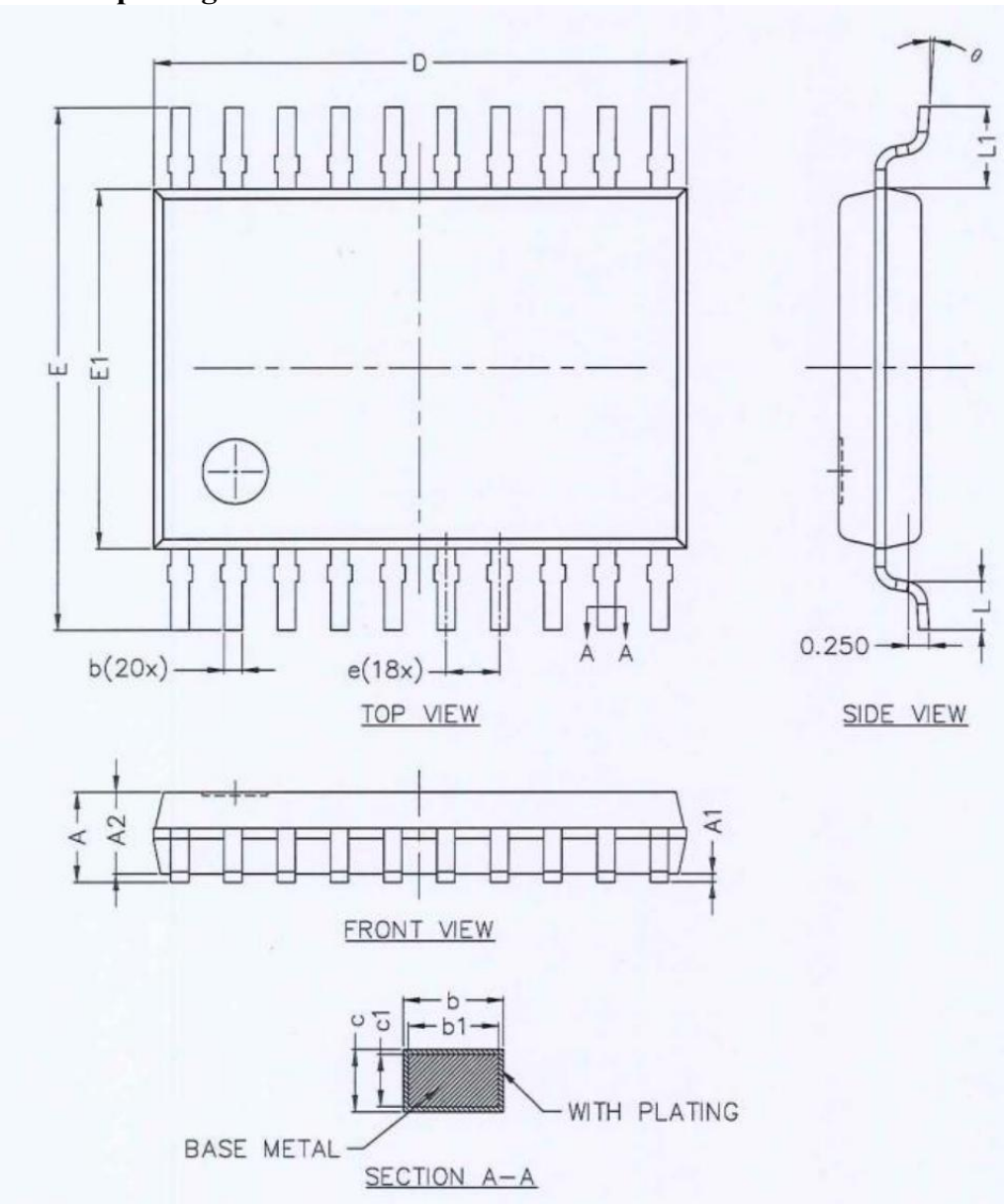
Symbol	Parameter	Min	Typical	Max	Unit
VDDA	Voltage Range	1.8	—	3.6	V
CMIR	Common Mode Input Range	0	—	VDDA	V
VIOFFSET	Input Offset Voltage	—	+-2	—	mV
ΔVIOFFSET	Input Offset Voltage Coefficient	—	+-34	—	uV/℃
TRIMOFFSETP	Input Offset Voltage Step Drive Current	—	4.4	9.96	mV
TRIMOFFSETN		—	4.5	10.49	
ILOAD(1)	Load Capacitance	—	—	500	uA
CLOAD(2)	Common Mode Rejection Ratio	—	—	50	pF
CMRR	Power Supply Rejection Ratio	—	60	—	dB
PSRR	CLOAD ≤ 50 pf, RLOAD ≥ 4 kΩ DC Vcom = VDDA/2	—	80	—	dB

GBW	Gain Bandwidth Product	—	17	20.2	MHz
SR	Input Voltage Conversion Rate (Normal Mode)	—	13.7	15.7	V/us
	Input Voltage Conversion Rate (High-Speed Mode)	—	28.5	30.6	
AO	Open Loop Gain 100mV ≤ Output Dynamic Range ≤ VDDA -100mV	65	95	—	dB
	Open Loop Gain 200mV ≤ Output dynamic range ≤ VDDA -200mV	75	95	—	
VOHSAT	Output High Saturation Voltage	VDDA-100	—	—	mV
VOLSAT	Output Low Saturation Voltage	—	—	100	mV
tWAKEUP	Wake-Up Time (Normal Mode)	—	2.2	2.2	us
	Wake-Up Time (High-Speed Mode)	—	2	2	
IDDA(OPA)	Normal Mode	—	380	407	uA
	High-Speed Mode	—	780	812	

1. Test with a 500uA load at the op-amp output.
2. Test with a 50pF load capacitance at the op-amp output.

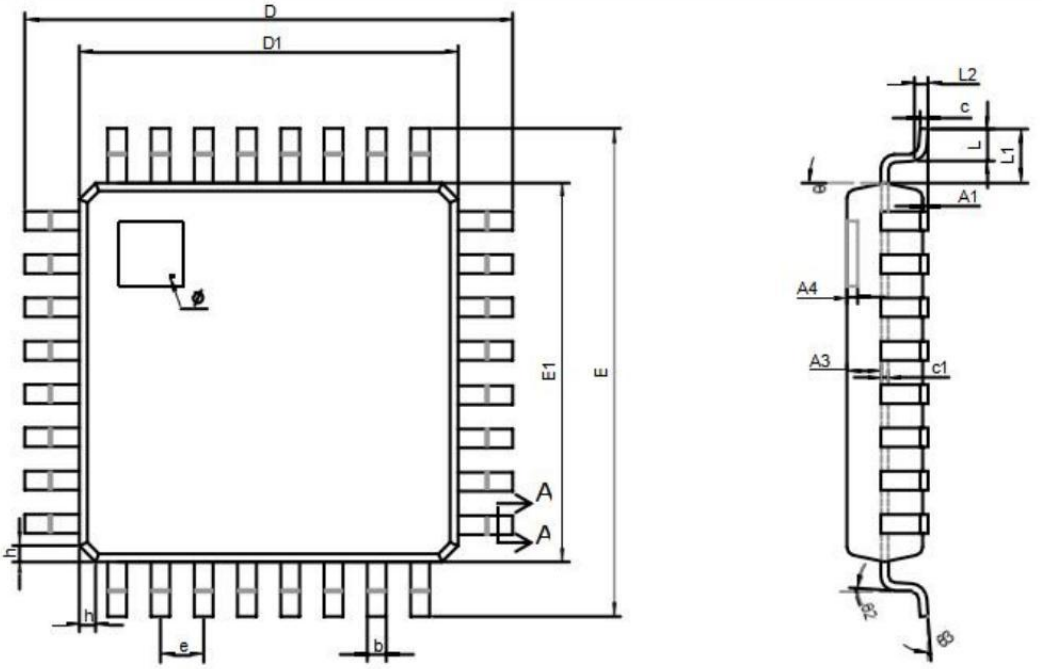
5 Package Features

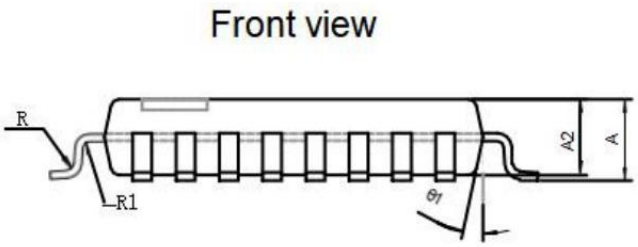
TSSOP20 package

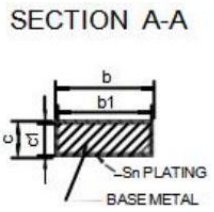


	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	–	–	1.20
STAND OFF	A1	0.05	0.100	0.15
MOLD TOTAL THICKNESS	A2	0.90	1.00	1.05
LEAD WIDTH–1	b	0.20	–	0.28
LEAD WIDTH–2	b1	0.19	0.22	0.25
LEAD THICKNESS–1	c	0.13	–	0.17
LEAD THICKNESS–2	c1	0.120	0.127	0.14
MOLD LENGTH	D	6.40	6.50	6.60
LEAD SPAN	E	6.20	6.40	6.60
MOLD WIDTH	E1	4.30	4.40	4.50
LEAD PITCH	e	0.65 BSC		
LEAD LENGTH	L1	0.85	1.00	1.15
LEAD SOLE LENGTH	L	0.45	0.60	0.75
LEAD FORM ANGLE	θ	0°	–	8°

LQFP32 Package



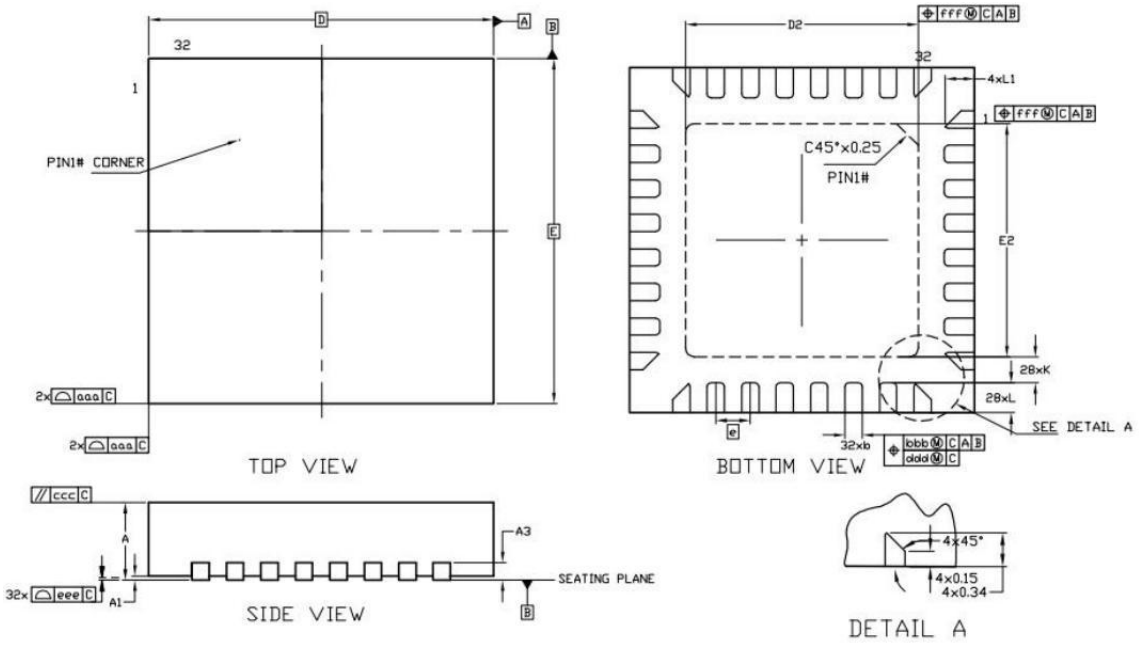




	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	-	-	1.60
STAND OFF	A1	0.05	0.10	0.20
BODY THICKNESS	A2	1.35	1.40	1.45
UP BODY THICKNESS	A3		0.64BSC	
THIMBLE DEPTH	A4	0.10	0.20	0.30
LEAD WIDTH	b	0.32	0.375	0.43
LEAD WIDTH	b1		0.35BSC	
L/F THICKNESS	C	0.127		0.16
L/F THICKNESS	c1	0.107	0.127	0.147
TOTAL SIZE X	D	8.80	9.00	9.20
BODY SIZE X	D1	6.90	7.00	7.10
TOTAL SIZE Y	E	8.80	9.00	9.20

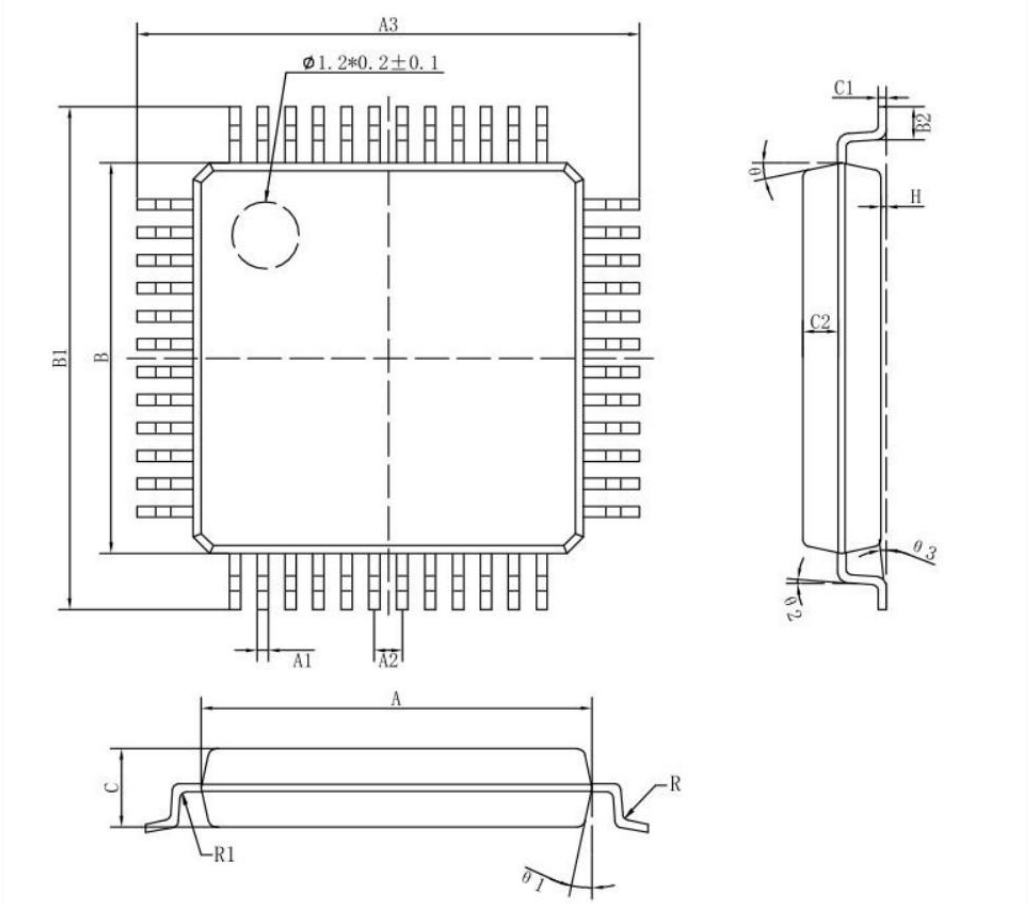
BODY SIZE Y	E1	6.90	7.00	7.10
LEAD PITCH	e	0.80BSC		
CHAMFER	h	0.20	0.30	0.40
FOOT LENGTH		0.45	0.65	0.75
LEAD LENGTH	L1	1.00BSC		
MEASURE POINT	L2	0.25BSC		
R RADIUS	R	0.15 REF		
R1 RADIUS	R1	0.12 REF		
ANGLE FOR MOLD	0	12*TYP		
ANGLE FOR MOLD	01	12*TYP		
ANGLE FOR LEAD	02	4° TYP		
ANGLE FOR FOOT	03	0* ~ 8*		
THIMBLE DIAMETER	0	1.10	1.20	1.30

QFN32 Package



DIM / SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
	0.80	0.85	0.90
A1	0	0.02	0.05
A3	–	0.20 REF	–
b	0.15	0.20	0.25
D		4.0BSC	
E		4.0BSC	
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.40BSC	
L	0.30	0.35	0.40
L1	0.29	0.34	0.39
K	0.20	–	–
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

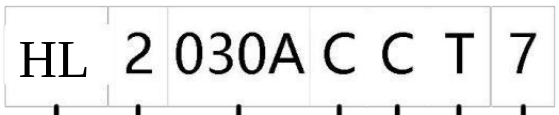
LQFP48 Package



尺寸 / 标注	最小(mm)	最大(mm)	尺寸 / 标注	最小(mm)	最大(mm)
A	6.90	7.10	C2	0.636TYP	
A1	0.20TYP		H	0.05	0.15
A2	0.50TYP		θ	12° TYP4	
A3	8.80	9.20	θ1	12° TYP4	
B	6.90	7.10	θ2	4° TYP	
B1	8.80	9.20	θ3	0° ～ 5°	
B2	0.50	0.80	R	0.15TYP	
C	1.30	1.50	R1	0.12TYP	
C1	0.127	0.16			

***(标注=mark 尺寸=size 最小=minimum 最大=maximum)**

6 Ordering Code



Product Lines

HL = **32 bits Micro Controller based on ARM**

Product Lines

2= Universal Type

Product Sublines

030A= Basic Typ

Number of pins

F=20pins

K=32pins

C=48pins

Storage Capacity

8 = 64K Flash + 16K Sram

B = 128K Flash + 32K Sram

C = 256K Flash + 32K Sram

Packaging information

P = TSSOP

T = LQFP

V = QFN(4x4)

Temperature

6 = -40~85°C

7 = -40~105°C

7 Version History

Version	Change Information
V1.0	Initial version
V1.1	Modified feature description and package info

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