Datasheet

HL2103Axxxx

Enhanced, True Random Number, Hardware Encryption Algorithm Unit, 32-bit MCU with 128 or 1024KB Flash, USB, CAN, 17 Timers, 3 ADCs, 2 DACs, 15 com. interfaces

Features:

- Core: 32-bit processor core
  - Up to 216MHz operation frequency, 2.54DMips/MHz(CoreMark1.0)
  - Single-cycle multiplication and hardware division
- Memories
  - 128K/256K/512K/1024K bytes of Flash memory
  - 32K/64K/96Kbytes of SRAM
  - FSMC Static memory controller
- Clock, reset and supply management
  - 2.0 ~ 3.6V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 4 ~ 16MHz crystal oscillator
  - Internal 8MHz factory-trimmed RC
  - Internal 40kHz RC oscillator with calibration
  - 32kHz RTC oscillator with calibration
- Low-power
  - Sleep, Stop and Standby modes
  - supply for RTC and backup registers
- 3 x 12-bit, 1 µs A/D converters (up to 21 channels)
  - Conversion range: 0 to 3.6V
  - Temperature sensor
- 2 x 12-bit D/A converters
- DMA： 12-channel DMA controller
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Embedded Tracking Module(ETM)
- I/O ports
  - 112 multi-function bidirectional I/O ports, all mappable on 16 external interrupts
  - All GPIOs can be forced to configure pull-up and pull-down resistors
- Enhanced CRC calculation unit
- 17 Timers
  - 10 x 16-bit timers, each with up to 4 input capture/output compare/PWM or pulse counter and quadrature (incremental) encoder input
  - 2 x 16-bit, advanced motor control PWM timer with dead-time generation and emergency stop
  - 2 watchdog timers (Independent and Window)
  - SysTick timer 24-bit downcounter
  - 2 x 16-bit base timers
- Up to 15 communication interface
  - Up to 2 x I2C interfaces(support SMBus/PMBus)
  - Up to 5 x USARTs interfaces(support ISO7816, LIN, IrDA capability and modem control)
  - Up to 3 x SPIs， 2 ofwhich are multiplexed with I2S interface
  - CAN interface(2.0B Active)
  - USB 2.0 full-speed interface(Optional internal 1.5K pull-up resistor)
  - SDIO interface
- Hardware encryption algorithm unit
  - Built-in hardware algorithm(DES、AES、SHA、SM1、SM3、SM4、SM7)
  - Provide a complete high-performance algorithm library
- TRNG：generate sequence oftrue random numbers
  - Four independent true random sources, which can be configured individually
  - 128BIT random numbers can be generated at one time
  - Optional digital post-processing function
  - Attack detection
- SENSOR：voltage & temperature sensor alarm
  - VBAT and VDD voltage can be detected independently
  - Provide temperature detection sensor
  - Optional reset or interrupt after alarm
- SRAM scrambling
  - Support address and data scrambling
- One Time Programmable (OTP)
  - Support 32 Byte

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1 Introduction

This datasheet includes: the basic configuration of HL2103Axxxx(such as the capacity of built-in Flash and RAM, the type and quantity of peripheral modules, etc.), the number and assignment of pins, electrical characteristics, package information, and ordering codes.

2 Specification

2.1 Device overview

Table 1 Device features and peripheral counts

Family		HL2103A						
Model		CBT6	CCT6	RPT6	VET6	VGT6	ZET6	ZGT6
Flash(Kbytes)		128	256	256	512	1024	512	1024
SRAM(Kbytes)		32	64	96	96	96	96	96
Timers	Advanced	1	1	2	2	2	2	2
	General-purpose	4	4	10	10	10	10	10
	Basic	2	2	2	2	2	2	2
Communication	SPI	3	3	3	3	3	3	3
	I2S	-	-	2	2	2	2	2
	I2C	2	2	2	2	2	2	2
	USART/UART	3	3	5	5	5	5	5
	USB	1	1	1	1	1	1	1
	CAN	1	1	1	1	1	1	1
	SDIO	-	-	1	1	1	1	1
FSMC		-	-	-	1	1	1	1
GPIO PORT		37	37	51	80	80	112	112
12 位 ADC (number of channels)		2(10channels)	2(10channels)	3(16channels)	3(16channels)	3(16channels)	3(21channels)	3(21channels)
12 位 DAC (number of channels)		2(2channels)	2(2channels)	2(2channels)	2(2channels)	2(2channels)	2(2channels)	2(2channels)
True Random Number Module		Support						
Hardware Encryption Algorithm Unit		Support						
Page size (Kbytes)		1	2	2	2	4	2	4
CPU frequency		216M						
Operating voltage		2.0~3.6V						
Operating temperature		–40 to +85°C						
Packages		LQFP48		LQFP64	LQFP100		LQFP144	

Introduction

2.1.1 32-bit RISC core with embedded Flash and SRAM

The 32-bit Core has been developed to provide a low-cost platform that meets the needs ofMCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

2.1.2 Embedded Flash memory

embedded Flash is available for storing programs and data.

Table 2 Supply voltage and Flash Delay level matching relationship

Flash Delay Level	HCLK(MHz)	
	Voltage Range	Voltage Range
	2.3V - 3.6V	2.0V - 2.3V
0	0 < HCLK <= 108	0 < HCLK <= 32
1	108 < HCLK <= 216	32 < HCLK <= 64
2	-	64 < HCLK <= 128
3	-	128 < HCLK <= 192
4	-	192 < HCLK <= 216

2.1.3 Memory Protection Unit(MPU)

The Memory Protection Unit (MPU) manages CPU access to memory, preventing one task from accidentally corrupting memory or resources used by another active task. This memory area is organized into up to 8 protected areas, which can in turn be subdivided into up to 8 sub-areas. The protected area size can range from 32 bytes to the entire 4 Gbytes ofaddressable memory.

MPUs are especially useful in applications where some critical or certified code must be protected from misbehavior by other tasks. It is usually managed by RTOS (RealTime Operating System). If a program accesses a memory location that is disabled by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the settings ofthe MPU area based on the executing process.

2.1.4 Embedded SRAM

Maximum 96 Kbytes ofembedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.1.5 Flexible Static Memory Controller(FSMC)

Support mode： PC card / Flash memory, SRAM, PSRAM, NOR and NAND.
Function overview：
- The three FSMC interrupt line passes through logic or is connected to the NVIC unit
- Write to FIFO
- Execute code from external memory other than NAND flash and PC cards

2.1.6 LCDParallel Port

FSMC can be configured to interface seamlessly with most graphics LCD controllers.It supports Intel 8080 and Motorola 6800 modes and is flexible enough to accommodate specific LCD interfaces.

2.1.7 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed polynomial (multiple modes optional and hardware data processing possible) generator.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.In the scope of the EN/IEC 60335-1 standard, it provides a means of detecting errors in flash memory.

2.1.8 Nested vectored interrupt controller (NVIC)

The HL2103Axxxx embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of the Core) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support interrupt tail-chaining function
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no extra instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.1.9 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.1.10 Clocks and startup

System clock selection is performed on startup, the internal RC 8 MHz oscillator is selected as default CPU clock on reset, then an external 4~32MHz clock with failure monitoring can be selected; when the external clock is detected to fail, it will be isolated. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed

APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 216MHz. The maximum allowed frequency of the low-speed APB domain is 108MHz.

2.1.11 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from program flash memory
- Boot from System Memory
- Boot from embedded SRAM

The Bootloader is located in System Memory. It is used to reprogram the Flash memory by using USART1.

2.1.12 Power supply schemes

- VDD: Power supply for I/Opins and internal voltage regulator.
- VSSA, VDDA: Provide power for analog part of ADC, reset module, RC oscillator and PLL. VDDA and VSSA must be connected to VDD and VSS, respectively.
- VBAT:Power supply for RTC, external clock 32 kHz oscillator and backup registers (through internal power switch) when VDD is not present.

Note: Refer to Table 9 for general operating conditions for each voltage range

2.1.13 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures that the system works when the power supply exceeds 2V. The device remains in reset mode when VDD is below a specified threshold, VPOR/PDR, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the VDD/VDDA power supply and compares it to the VPVD threshold. An interrupt can be generated when VDD/VDDA is below or above the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCUinto a safe state. The PVD is enabled by software.

2.1.14 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the stop mode of CPU
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

2.1.15 Low-power modes

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

The Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. The power supply of all internal 1.1V parts is stopped, the PLL, HSIRC oscillator and HSE crystal oscillator are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.

- Standby mode

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.1V domain is powered off.The PLL, the HSIRC and the HSE crystal oscillators are also switched off.After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry. The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.1.16 DMA

Supports up to 12 general-purpose DMAs (7channels for DMA1, 5channels for DMA2) to manage memory-to-memory, device-to-memory, and memory-to-device data transfers; The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent. The DMA can be used with the main peripherals: SPI/I2S, I2C, USART, advanced/General/Basic timers TIMx, ADC, DAC and SDIO.

2.1.17 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on VDD supply when present or through the VBATpin. The backup registers (forty-two 16-bit registers) can be used to store 84 bytes of user application data when VDD power is not present. The RTC and backup registers are not reset by system or power reset sources; nor are they reset when waking up from standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. RTCis clocked by a 32.768kHz oscillator using an external crystal, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-power RC has a typical frequency of40kHz. The RTC can be calibrated using an external 512Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long-term measurement using the compare register. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768kHz.

2.1.18 Timers and watchdogs

HL2103A series include at most 2 advanced-control timers, 10 general-purpose timers, 2 basic timers, 2 watchdog timers and 1 SysTick timer.

Below table compares the features ofthe advanced-control, general-purpose and basic timers.

Table 3 TIM configuration

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1 TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2 TIM3 TIM4 TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9 TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM10 TIM11 TIM13 TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6 TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timer (TIM1 and TIM8)

Two advanced-control timers (TIM1 and TIM8) can be seen as two three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

Ifconfigured as a general-purpose 16-bit timer, it has the same features as the TIMx timer. Ifconfigured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the counter can be frozen and the PWM outputs disabled to turn offany power switch driven by these outputs.

Many features are shared with those ofthe general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timer(TIM2、TIM3、TIM4、TIM5)

There are up to four synchronizable general-purpose timers embedded in the HL2103Axxxx devices.These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and 4 independent channels each for input capture/output compare, PWM or single-pulse mode output. The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are also capable of processing incremental encoder signals as well as digital outputs from 1 to 3 hall-effect sensors.

General-purpose timer(TIM10、TIM11、TIM9)

These timers are based on a 16-bit auto-reload counter and a 16-bit prescaler. TIM10 and TIM11 have one independent channel, while TIM9 has two independent channel outputs for input capture/output compare, PWM or single-pulse mode. They can fully synchronize general purpose timers with TIM2, TIM3, TIM4, TIM5. They can also be used as a simple time base.

General-purpose timer(TIM13、TIM14、TIM12)

These timers are based on a 16-bit auto-reload counter and a 16-bit prescaler. TIM13 and TIM14 have one independent channel, while TIM12 has two independent channels outputs for input capture/output compare, PWM or single-pulse mode. They can fully synchronize general purpose timers with TIM2, TIM3, TIM4, TIM5. They can also be used as a simple time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40kHz internal RC and as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the system when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

Basic timer TIM6 and TIM7

These timers are mainly used for the generation of DAC triggers. They can also be used as a universal 16-bit time base.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the system when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0

● Programmable clock source

2.1.19 I2C bus

Up to two I2C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes. The I2Cinterface supports 7-bit or 10-bit addressing, and the 7-bit slave mode supports dual-slave addressing. A hardware CRC generation /verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

2.1.20 Universal synchronous/asynchronous receiver transmitter (USART)

Three universal synchronous/asynchronous receiver transmitter(USART1, USART2 and USART3) and two universal asynchronous receiver transmitter(UART4和UART5).The five interfaces provide asynchronous communication, IrDA SIRENDEC support,Multi-processor communication mode, single-line semi-duplex communication mode and LIN Master/Slave capability.

USART1 interface communication rate can reach 13.5Mbits/s.

USART1, USART2 and USART3 provide hardware management of the CTS and RTS signals, are compliant with ISO7816 smart card mode and SPI-like communication mode.

2.1.21 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 30Mbits/s in slave and master modes in full duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

2.1.22 Audio interface (I2S)

Two standard I S interfaces (multiplexed with SPI2 and SPI3) can be operated in the master or slave mode, which can be configured to 16-bit or 32-bit transmission, can also be configured as input or output channels, support audio sampling frequency from 8kHz to 48kHz. When either one or two I2S interfaces are configured as the master mode, its main clock can be output to the external DAC or CODEC (decoder) at 256 times the sample frequency.

2.1.23 SDIO

The SD/SDIO/MMC host interface can support 3 different data bus modes in the MMC Card System Specification 4.2: 1-bit (default), 4-bit, and 8-bit. SDIO Memory Card Specification 2.0 supports two data bus modes: 1-bit (default) and 4-digit. The current chip version can only support an SD/ SDIO/MMC version 4.2 card, but can support multiple MMC version 4.1 or previous versions of cards.

In addition to SD/SDIO/MMC, this interface is fully compliance with the CE-ATA Digital Protocol version1.1.

2.1.24 Controller area network (CAN)

The CAN is compliance with specifications 2.0A and 2.0B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.1.25 Universal serial bus (USB)

Embedded a full-speed USB device controller, follows the full-speed USB device (12m/s) standard. The endpoint can be configured by software, standby/wake-up features. The USB dedicated 48MHz clock is directly generated by the internal master PLL (the clock source can be arbitrary).

2.1.26 General-purpose inputs/outputs(GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable, except for ports with analog input capabilities.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Each I/O can be configured with forced pull-up and pull-down resistors to save external resistor consumption.

2.1.27 Analog-to-digital converter(ADC)

Up to three 12-bit analog-to-digital converters(ADC) are embedded into HL2103Axxxx and each ADC shares up to 16 external channels, performing conversions in singleshot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface include:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1 and TIM8) can be internally connected to the ADC start trigger and injection trigger respectively, to allow the application to synchronize A/D conversion and timers.

2.1.28 Digital-to-analog converter(DAC)

Two 12-bit buffered DAC channels can be used to convert 2-channel digital signals into 2-channel analog voltage signals and output. This dual digital interface supports the following functions:

- Two DAC converters: each has one output channel

- 8-bit or 12-bit monotonic output
- Left and right data alignment in 12-bit mode
- Synchronous update function
- Generates noise waves
- Generate triangular waves
- Dual DAC channel independent or simultaneous conversion
- Each channel can use DMA function
- External trigger for conversion
- Input reference voltage V REF+

The DAC channel can be triggered by the update output ofthe timer, which can also be connected to a different DMA channel.

2.1.29 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC11_IN16 input channel which is used to convert the sensor output voltage into a digital value

2.1.30 Serial wire JTAG debug port(SWJ-DP)

The embedded SWJ-DP interface is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.1.31 Embedded Tracking Module(ETM)

Using embedded tracking module(ETM), connected to external tracking port analysis (TPA) devices through very few ETM pins, it outputs compressed data flow at high speed from the CPU core, providing developers with clear information about instruction running and data flow.TPA devices can be connected to the debugging host via USB, Ethernet, or other high-speed channels. The real-time instructions and data flow direction can be recorded by the debugging software on the debugging host and displayed in the required format.The TPA hardware is available from development tool vendors and is compliance with third-party debugging software.

2.1.32 True random number generator(TRNG)

The TRNG units are used to generate sequences of true random numbers.One-time work produces a sequence of 128-bit true random numbers.Random numbers can be configured to generate a CPU interrupt request.

3 Pinouts and pin description

LQFP48 package

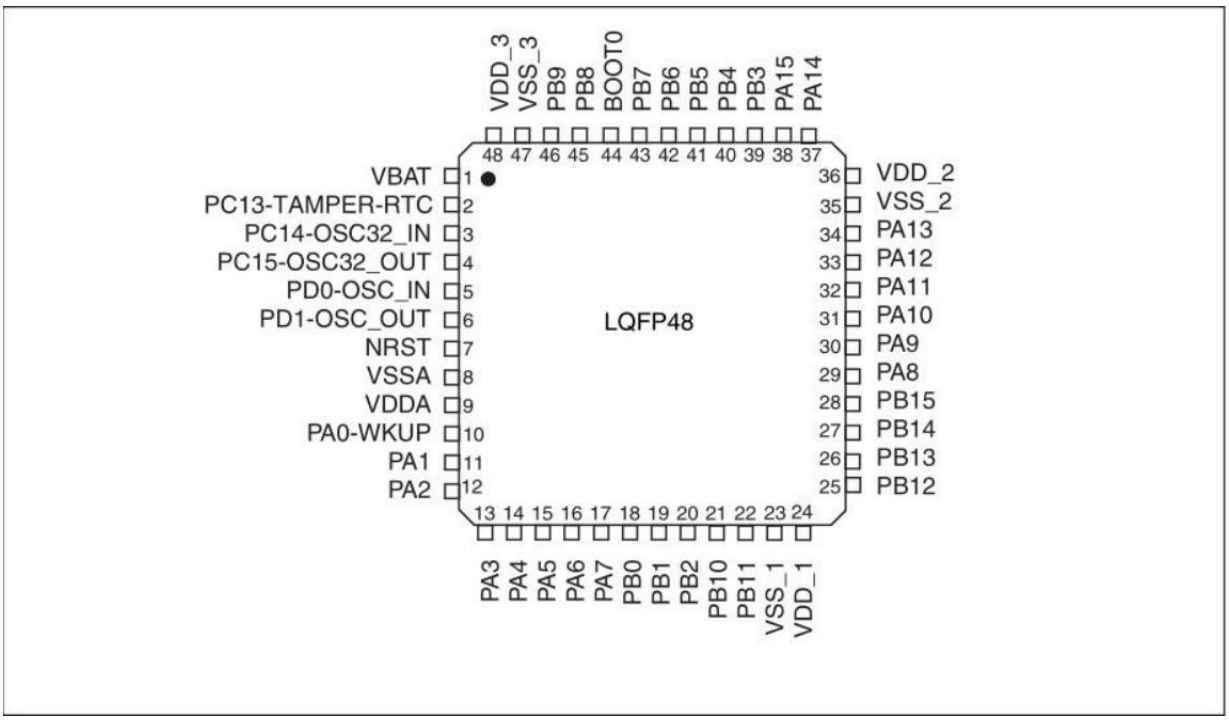


Figure 1 LQFP48 package

LQFP64 package

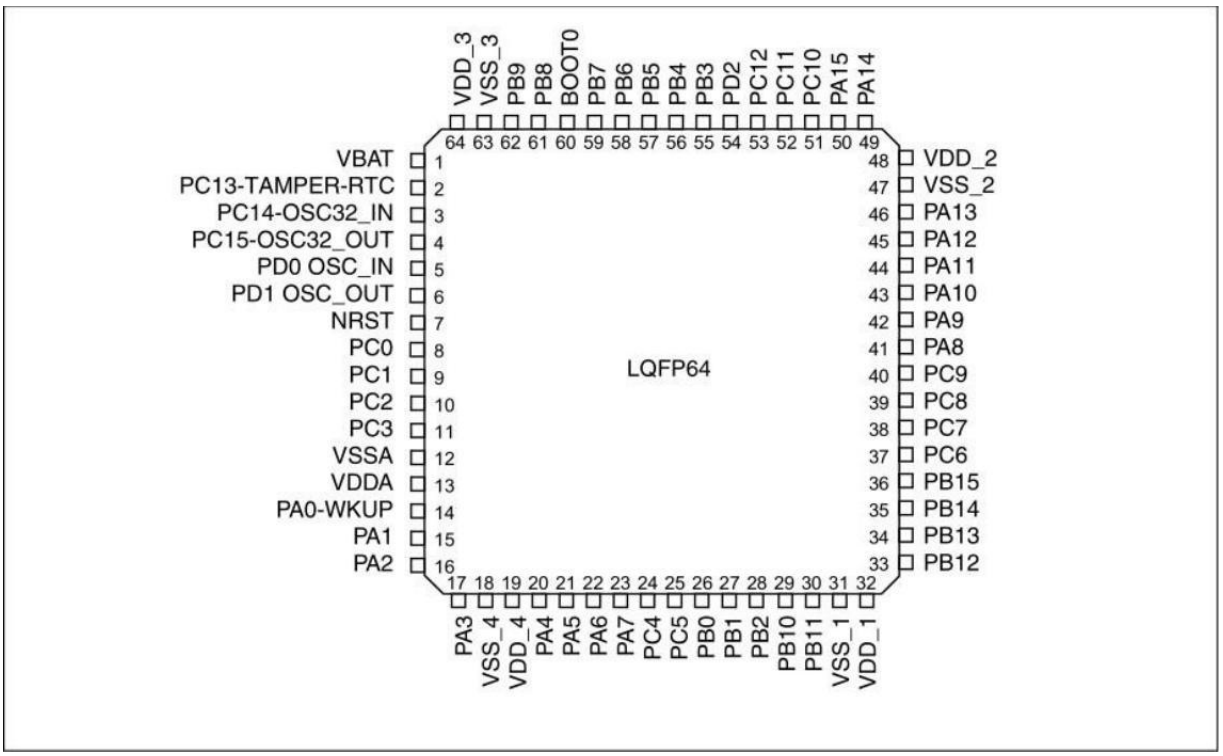


Figure 2 LQFP64 package

LQFP100 package

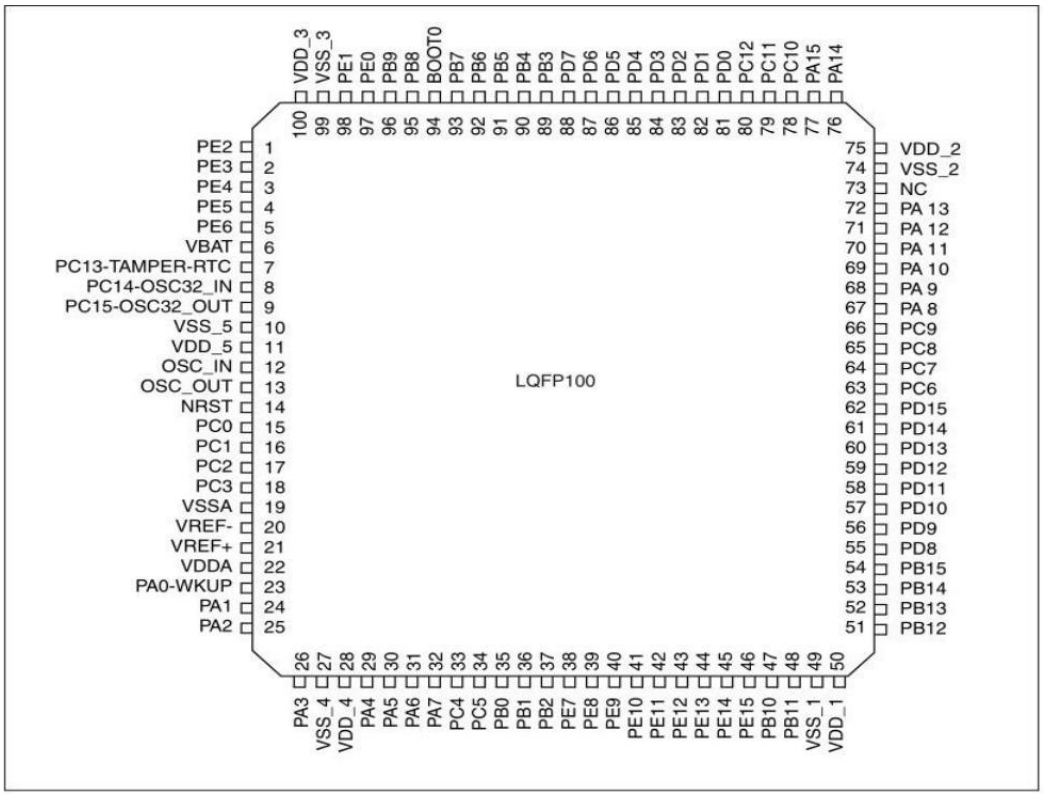


Figure3 LQFP100 package

LQFP144 package

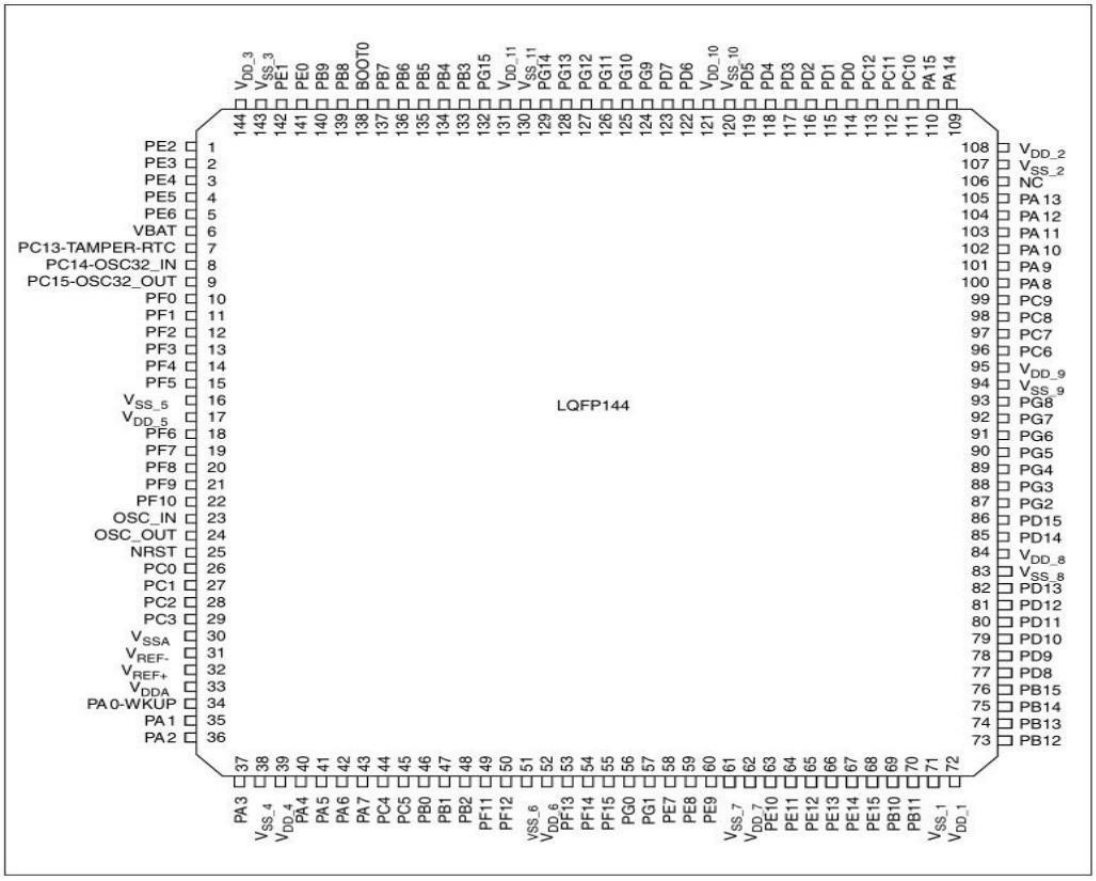


Figure4 LQFP144 package

LQFP48 pin definition

Table 4 LQFP 48 pin definition

LQFP 48	Pin Name	Type	I/O Level	Main Function (after reset)	Default	Remap
1	VBAT	S	_	VBAT	_	_
2	PC13-TAMPERRTC	I/O	_	PC13	TAMPER-RTC	_
3	PC14-OSC32_IN	I/O	_	PC14	OSC32_IN	_
4	PC15-OSC32_OUT	I/O	_	PC15	OSC32_OUT	_
5	OSC_IN	I/O	_	OSC_IN	_	PD0
6	OSC_OUT	I/O	_	OSC_OUT	_	PD1
7	NRST	I/O	_	NRST	-	-
8	VSSA	S	_	VSSA	-	-
9	VDDA	S	_	VDDA	-	-
10	PA0-WKUP	I/O	_	PA0	WKUP/USART2_CTS/ ADC12_IN0/TIM2_CH1_ETR/ TIM5_CH1	-
11	PA1	I/O	_	PA1	USART2_RTS/ADC12_IN1/ TIM2_CH2/TIM5_CH2	-
12	PA2	I/O	_	PA2	USART2_TX/ADC12_IN2/ TIM2_CH3/TIM5_CH3/	-
13	PA3	I/O	_	PA3	USART2_RX/ADC12_IN3/ TIM2_CH4/TIM5_CH4/	-
14	PA4	I/O	_	PA4	SPI1_NSS/USART2_CK/ DAC_OUT1/ADC12_IN4	-
15	PA5	I/O	_	PA5	SPI1_SCK/ADC12_IN5/ DAC_OUT2	-
16	PA6	I/O	_	PA6	SPI1_MISO/ADC12_IN6/ TIM3_CH1	TIM1_BKIN
17	PA7	I/O	_	PA7	SPI1_MOSI/ADC12_IN7/ TIM3_CH2	TIM1_CH1N
18	PB0	I/O	_	PB0	ADC12_IN8/TIM3_CH3	TIM1_CH2N
19	PB1	I/O	_	PB1	ADC12_IN9/TIM3_CH4	TIM1_CH3N
20	PB2	I/O	FT	PB2/BOOT1	-	-
21	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX	TIM2_CH3
22	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX	TIM2_CH4
23	VSS_1	S	_	VSS_1	_	_
24	VDD_1	S	_	VDD_1	_	_
25	PB12	I/O	FT	PB12	SPI2_NSS/I2C2_SMBA/ USART3_CK/TIM1_BKIN	_
26	PB13	I/O	FT	PB13	SPI2_SCK/USART3_CTS/ TIM1_CH1N	_
27	PB14	I/O	FT	PB14	SPI2_MISO/USART3_RTS/ TIM1_CH2N	_
28	PB15	I/O	FT	PB15	SPI2_MOSI/TIM1_CH3N	_

29	PA8	I/O	FT	PA8	USART1_CK/TIM1_CH1/ MCO	_
30	PA9	I/O	FT	PA9	USART1_TX/TIM1_CH2	_
31	PA10	I/O	FT	PA10	USART1_RX/TIM1_CH3	_
32	PA11	I/O	-	PA11	USART1_CTS/USBDM CAN_RX/TIM1_CH4	_
33	PA12	I/O	-	PA12	USART1_RTS/USBDP/ CAN_TX/TIM1_ETR	_
34	PA13	I/O	FT	JTMS-SWDIO	_	PA13
35	VSS_2	S	_	VSS_2	_	_
36	VDD_2	S	_	VDD_2	_	_
37	PA14	I/O	FT	JTCK-SWCLK	_	PA14
38	PA15	I/O	FT	JTDI	SPI3_NSS	TIM2_CH1_ETR/ PA15/ SPI1_NSS
39	PB3	I/O	FT	JTDO	SPI3_SCK	TIM2_CH2/PB3/TRACESWO/SPI1_SCK
40	PB4	I/O	FT	NJTRST	SPI3_MISO	TIM3_CH1/PB4/ SPI1_MISO
41	PB5	I/O	_	PB5	I2C1_SMBA/ SPI3_MOSI	TIM3_CH2/ SPI1_MOSI
42	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
43	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2	USART1_RX
44	BOOT0	I	_	BOOT0	-	-
45	PB8	I/O	FT	PB8	TIM4_CH3	I2C1_SCL/CAN_RX
46	PB9	I/O	FT	PB9	TIM4_CH4	I2C1_SDA/CAN_TX
47	VSS_3	S	_	VSS_3	-	-
48	VDD_3	S	_	VDD_3	-	-

(1) FT = 5V tolerant

LQFP64 pin definition

Table 5 LQFP 64p in definition

LQFP 64	Pin Name	Type	I/O Level	Main Function (after reset)	Default	Remap
1	VBAT	S	_	VBAT	-	-
2	PC13-TAMPERRTC	I/O	_	PC13	TAMPER-RTC	-
3	PC14-OSC32_IN	I/O	_	PC14	OSC32_IN	PD0
4	PC15-OSC32_OUT	I/O	_	PC15	OSC32_OUT	PD1
5	OSC_IN	I/O	_	OSC_IN	-	-
6	OSC_OUT	I/O	_	OSC_OUT	-	-
7	NRST	I/O	_	NRST	-	-
8	PC0	I/O	_	PC0	ADC123_IN10	-
9	PC1	I/O	_	PC1	ADC123_IN11	-
10	PC2	I/O	_	PC2	ADC123_IN12	-
11	PC3	I/O	_	PC3	ADC123_IN13	-
12	VSSA	S	_	VSSA	-	-
13	VDDA	S	_	VDDA	-	-

14	PA0-WKUP	I/O	_	PA0	WKUP/USART2_CTS/ ADC123_IN0/TIM2_CH1_ETR/ TIM5_CH1/TIM8_ETR	-
15	PA1	I/O	_	PA1	USART2_RTS/ADC123_IN/ TIM2_CH2/TIM5_CH2	-
16	PA2	I/O	_	PA2	USART2_TX/ADC123_IN2/ TIM2_CH3/TIM5_CH3/ TIM9_CH1	-
17	PA3	I/O	_	PA3	USART2_RX/ADC123_IN3/ TIM2_CH4/TIM5_CH4/ TIM9_CH2	-
18	VSS_4	S	_	VSS_4	-	-
19	VDD_4	S	_	VDD_4	-	-
20	PA4	I/O	_	PA4	SPI1_NSS/USART2_CK/ DAC_OUT1/ADC12_IN4	-
21	PA5	I/O	_	PA5	SPI1_SCK/ADC12_IN5/ DAC_OUT2	-
22	PA6	I/O	_	PA6	SPI1_MISO/ADC12_IN6/ TIM3_CH1/TIM8_BKIN/ TIM13_CH1	TIM1_BKIN
23	PA7	I/O	_	PA7	SPI1_MOSI/ADC12_IN7/ TIM3_CH2/TIM8_CH1N/ TIM14_CH1	TIM1_CH1N
24	PC4	I/O		PC4	ADC12_IN14	-
25	PC5	I/O		PC5	ADC12_IN15	-
26	PB0	I/O	_	PB0	ADC12_IN8/TIM3_CH3/ TIM8_CH2N	TIM1_CH2N
27	PB1	I/O	_	PB1	ADC12_IN9/TIM3_CH4/ TIM8_CH3N	TIM1_CH3N
28	PB2	I/O	FT	PB2/BOOT1	-	-
29	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX	TIM2_CH3
30	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX	TIM2_CH4
31	VSS_1	S	_	VSS_1	-	-
32	VDD_1	S	_	VDD_1	-	-
33	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/ I2C2_SMBA/USART3_CK/ TIM1_BKIN	-
34	PB13	I/O	FT	PB13	SPI2_SCK/I2S2_CK/ USART3_CTS/TIM1_CH1N	-
35	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS/TIM12_CH1	-
36	PB15	I/O	FT	PB15	SPI2_MOSI/I2S2_SD/ TIM1_CH3N/TIM12_CH2	-
37	PC6	I/O	FT	PC6	I2S2_MCK/TIM8_CH1/ SDIO_D6	TIM3_CH1
38	PC7	I/O	FT	PC7	I2S3_MCK/TIM8_CH2/ SDIO_D7	TIM3_CH2
39	PC8	I/O	FT	PC8	TIM8_CH3/SDIO_D0	TIM3_CH3
40	PC9	I/O	FT	PC9	TIM8_CH4/SDIO_D1	TIM3_CH4
41	PA8	I/O	FT	PA8	USART1_CK/TIM1_CH1 / MCO	-
42	PA9	I/O	FT	PA9	USART1_TX/TIM1_CH2	-
43	PA10	I/O	FT	PA10	USART1_RX/TIM1_CH3	-
44	PA11	I/O	-	PA11	USART1_CTS/USBDM CAN_RX/TIM1_CH4	-

45	PA12	I/O	-	PA12	USART1_RTS/USBDP/ CAN_TX/TIM1_ETR	-
46	PA13	I/O	FT	JTMS-SWDIO	-	PA13
47	VSS_2	S	_	VSS_2	-	-
48	VDD_2	S	–	VDD_2	-	-
49	PA14	I/O	FT	JTCK-SWCLK	-	PA14
50	PA15	I/O	FT	JTDI	SPI3_NSS/I2S3_WS	TIM2_CH1_ETR/ PA15/ SPI1_NSS
51	PC10	I/O	FT	PC10	UART4_TX/SDIO_D2	USART3_TX
52	PC11	I/O	FT	PC11	UART4_RX/SDIO_D3	USART3_RX
53	PC12	I/O	FT	PC12	UART5_TX/SDIO_CK	USART3_CK
54	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX SDIO_CMD	
55	PB3	I/O	FT	JTDO	SPI3_SCK/I2S3_CK	PB3/TRACESWO TIM2_CH2/SPI1_SCK
56	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4/TIM3_CH1/ SPI1_MISO
57	PB5	I/O	_	PB5	I2C1_SMBA/SPI3_MOSI /I2S3_SD	TIM3_CH2/SPI1_MO SI
58	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
59	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2	USART1_RX
60	BOOT0	I	_	BOOT0	-	_
61	PB8	I/O	FT	PB8	TIM4_CH3/SDIO_D4/ TIM10_CH1	I2C1_SCL/CAN_RX
62	PB9	I/O	FT	PB9	TIM4_CH4/SDIO_D5/ TIM11_CH1	I2C1_SDA/CAN_TX
63	VSS_3	S	_	VSS_3	-	-
64	VDD_3	S	_	VDD_3	-	-

(1) FT = 5V tolerant

LQFP100 pin definition

Table 6 LQFP100 pin definition

LQFP 100	Pin Name	Type	I/O Level	Main Function (after reset)	Default	Remap
1	PE2	I/O	FT	PE2	FSMC_A23	-
2	PE3	I/O	FT	PE3	FSMC_A19	-
3	PE4	I/O	FT	PE4	FSMC_A20	-
4	PE5	I/O	FT	PE5	FSMC_A21	-
5	PE6	I/O	FT	PE6	FSMC_A22	-
6	VBAT	S	_	VBAT	-	-
7	PC13-TAMPERRTC	I/O	–	PC13	TAMPER-RTC	-

8	PC14-OSC32_IN	I/O	_	PC14	OSC32_IN	-
9	PC15-OSC32_OUT	I/O	_	PC15	OSC32_OUT	-
10	VSS_5	S	_	VSS_5	_	
11	VDD_5	S	_	VDD_5	_	
12	OSC_IN	I	_	OSC_IN	-	-
13	OSC_OUT	O	_	OSC_OUT	-	-
14	NRST	I/O	_	NRST	-	-
15	PC0	I/O	_	PC0	ADC123_IN10	-
16	PC1	I/O	_	PC1	ADC123_IN11	-
17	PC2	I/O	_	PC2	ADC123_IN12	-
18	PC3	I/O	_	PC3	ADC123_IN13	-
19	VSSA	S	_	VSSA	-	-
20	Vref-	S	_	Vref-	-	-
21	Vref+	S	_	Vref+	-	-
22	VDDA	S	_	VDDA	-	-
23	PA0-WKUP	I/O	_	PA0	WKUP/USART2_CTS/ ADC123_IN0/TIM2_CH1_ETR/ TIM5_CH1/TIM8_ETR	-
24	PA1	I/O	_	PA1	USART2_RTS/ADC123_IN1/ TIM2_CH2/TIM5_CH2	-
25	PA2	I/O	_	PA2	USART2_TX/ADC123_IN2/ TIM2_CH3/TIM5_CH3/ TIM9_CH1	-
26	PA3	I/O	_	PA3	USART2_RX/ADC123_IN3/ TIM2_CH4/TIM5_CH4/ TIM9_CH2	-
27	VSS_4	S	_	VSS_4	-	-
28	VDD_4	S	_	VDD_4	-	-
29	PA4	I/O	_	PA4	SPI1_NSS/USART2_CK/ DAC_OUT1/ADC12_IN4	-
30	PA5	I/O	_	PA5	SPI1_SCK/ADC12_IN5/ DAC_OUT2	-
31	PA6	I/O	_	PA6	SPI1_MISO/ADC12_IN6/	TIM1_BKIN

					TIM3_CH1/TIM8_BKIN/ TIM13_CH1	
32	PA7	I/O	–	PA7	SPI1_MOSI/ADC12_IN7/ TIM3_CH2/TIM8_CH1N/ TIM14_CH1	TIM1_CH1N
33	PC4	I/O		PC4	ADC12_IN14	-
34	PC5	I/O		PC5	ADC12_IN15	-
35	PB0	I/O	_	PB0	ADC12_IN8/TIM3_CH3/ TIM8_CH2N	TIM1_CH2N
36	PB1	I/O	_	PB1	ADC12_IN9/TIM3_CH4/ TIM8_CH3N	TIM1_CH3N
37	PB2	I/O	FT	PB2/BOOT1	-	-
38	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
39	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
40	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
41	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
42	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
43	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
44	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
45	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
46	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
47	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX	TIM2_CH3
48	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX	TIM2_CH4
49	VSS_1	S	_	VSS_1	-	-
50	VDD_1	S	_	VDD_1	-	-
51	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/ I2C2_SMBA/USART3_CK/ TIM1_BKIN	-
52	PB13	I/O	FT	PB13	SPI2_SCK/I2S2_CK/ USART3_CTS/TIM1_CH1N	-
53	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS/TIM12_CH1	-
54	PB15	I/O	FT	PB15	SPI2_MOSI/I2S2_SD/ TIM1_CH3N/TIM12_C	-

					H2	
55	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
56	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
57	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
58	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
59	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1/USART3_RX
60	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
61	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
62	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
63	PC6	I/O	FT	PC6	I2S2_MCK/TIM8_CH1 / SDIO_D6	TIM3_CH1
64	PC7	I/O	FT	PC7	I2S3_MCK/TIM8_CH2 / SDIO_D7	TIM3_CH2
65	PC8	I/O	FT	PC8	TIM8_CH3/SDIO_D0	TIM3_CH3
66	PC9	I/O	FT	PC9	TIM8_CH4/SDIO_D1	TIM3_CH4
67	PA8	I/O	FT	PA8	USART1_CK/TIM1_CH1/ MCO	-
68	PA9	I/O	FT	PA9	USART1_TX/TIM1_CH2	-
69	PA10	I/O	FT	PA10	USART1_RX/TIM1_CH3	-
70	PA11	I/O	-	PA11	USART1_CTS/USBDM CAN_RX/TIM1_CH4	-
71	PA12	I/O	-	PA12	USART1_RTS/USBDP / CAN_TX/TIM1_ETR	-
72	PA13	I/O	FT	JTMS-SWDIO	-	PA13
73	Not Connected					-
74	VSS_2	S	_	VSS_2	-	-
75	VDD_2	S	_	VDD_2	-	-
76	PA14	I/O	FT	JTCK-SWCLK	-	PA14
77	PA15	I/O	FT	JTDI	SPI3_NSS/I2S3_WS	TIM2_CH1_ETR/PA15/ SPI1_NSS

78	PC10	I/O	FT	PC10	UART4_TX/SDIO_D2	USART3_TX
79	PC11	I/O	FT	PC11	UART4_RX/SDIO_D3	USART3_RX
80	PC12	I/O	FT	PC12	UART5_TX/SDIO_CK	USART3_CK
81	PD0	I/O	FT	PD0	FSMC_D2	CAN_RX
82	PD1	I/O	FT	PD1	FSMC_D3	CAN_TX
83	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX SDIO_CMD	-
84	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
85	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
86	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
87	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
88	PD7	I/O	FT	PD7	FSMC_NE1/FSMC_NCE2	USART2_CK
89	PB3	I/O	FT	JTDO	SPI3_SCK/I2S3_CK	PB3/TRACESWO TIM2_CH2/SPI1_SCK
90	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4/TIM3_CH1/ SPI1_MISO
91	PB5	I/O	_	PB5	I2C1_SMBA/SPI3_MOSI /I2S3_SD	TIM3_CH2/SPI1_MOSI
92	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
93	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2 / FSMC_NADV	USART1_RX
94	BOOT0	I	_	BOOT0	-	_
95	PB8	I/O	FT	PB8	TIM4_CH3/SDIO_D4/ TIM10_CH1	I2C1_SCL/CAN_RX
96	PB9	I/O	FT	PB9	TIM4_CH4/SDIO_D5/ TIM11_CH1	I2C1_SDA/CAN_TX
97	PE0	I/O	FT	PE0	TIM4_ETR/FSMC_NBL0	-
98	PE1	I/O	FT	PE1	FSMC_NBL1	-
99	VSS_3	S	_	VSS_3	-	-
100	VDD_3	S	_	VDD_3	-	-

LQFP144 pin definition

Table 7 LQFP 144 pin definition

LQFP 144	Pin Name	Type	I/O Level	Main Function (after reset)	Default	Remap
1	PE2	I/O	FT	PE2	FSMC_A23	-
2	PE3	I/O	FT	PE3	FSMC_A19	-
3	PE4	I/O	FT	PE4	FSMC_A20	-
4	PE5	I/O	FT	PE5	FSMC_A21	-
5	PE6	I/O	FT	PE6	FSMC_A22	-
6	VBAT	S	_	VBAT	-	-
7	PC13-TAMPERRTC	I/O	_	PC13	TAMPER-RTC	-
8	PC14-OSC32_IN	I/O	_	PC14	OSC32_IN	-
9	PC15-OSC32_OUT	I/O	_	PC15	OSC32_OUT	-
10	PF0	I/O	FT	PF0	FSMC_A0	_
11	PF1	I/O	FT	PF1	FSMC_A1	_
12	PF2	I/O	FT	PF2	FSMC_A2	_
13	PF3	I/O	FT	PF3	FSMC_A3	_
14	PF4	I/O	FT	PF4	FSMC_A4	_
15	PF5	I/O	FT	PF5	FSMC_A5	_
16	VSS_5	S	_	VSS_5	_	_
17	VDD_5	S	_	VDD_5	_	_
18	PF6	I/O	_	PF6	ADC3_IN4/FSMC_NIORD	_
19	PF7	I/O	_	PF7	ADC3_IN5/FSMC_NREG	_
20	PF8	I/O	_	PF8	ADC3_IN6/FSMC_NIOWR	_
21	PF9	I/O	_	PF9	ADC3_IN7/FSMC_CD	_
22	PF10	I/O	_	PF10	ADC3_IN8/FSMC_INTR	_
23	OSC_IN	I	_	OSC_IN	-	-
24	OSC_OUT	O	_	OSC_OUT	-	-
25	NRST	I/O	_	NRST	-	-
26	PC0	I/O	_	PC0	ADC123_IN10	_
27	PC1	I/O	_	PC1	ADC123_IN11	_

28	PC2	I/O	_	PC2	ADC123_IN12	-
29	PC3	I/O	_	PC3	ADC123_IN13	-
30	VSSA	S	_	VSSA	-	-
31	Vref-	S	_	Vref-	-	-
32	Vref+	S	_	Vref+	-	-
33	VDDA	S	_	VDDA	-	-
34	PA0-WKUP	I/O	_	PA0	WKUP/USART2_CTS/ ADC123_IN0/TIM2_CH1_ETR/ TIM5_CH1/TIM8_ETR	-
35	PA1	I/O	_	PA1	USART2_RTS/ADC123_IN1/ TIM2_CH2/TIM5_CH2	-
36	PA2	I/O	_	PA2	USART2_TX/ADC123_IN2/ TIM2_CH3/TIM5_CH3/ TIM9_CH1	-
37	PA3	I/O	_	PA3	USART2_RX/ADC123_IN3/ TIM2_CH4/TIM5_CH4/ TIM9_CH2	-
38	VSS_4	S	_	VSS_4	-	-
39	VDD_4	S	_	VDD_4	-	-
40	PA4	I/O	_	PA4	SPI1_NSS/USART2_CK/ DAC_OUT1/ADC12_IN4	-
41	PA5	I/O	_	PA5	SPI1_SCK/ADC12_IN5/ DAC_OUT2	-
42	PA6	I/O	_	PA6	SPI1_MISO/ADC12_IN6/ TIM3_CH1/TIM8_BKIN/ TIM13_CH1	TIM1_BKIN
43	PA7	I/O	_	PA7	SPI1_MOSI/ADC12_IN7/ TIM3_CH2/TIM8_CH1N/ TIM14_CH1	TIM1_CH1N
44	PC4	I/O		PC4	ADC12_IN14	-
45	PC5	I/O		PC5	ADC12_IN15	-
46	PB0	I/O	_	PB0	ADC12_IN8/TIM3_CH	TIM1_CH2N

					3/ TIM8_CH2N	
47	PB1	I/O	–	PB1	ADC12_IN9/TIM3_CH4/ TIM8_CH3N	TIM1_CH3N
48	PB2	I/O	FT	PB2/BOOT1	-	-
49	PF11	I/O	FT	PF11	FSMC_NISO16	-
50	PF12	I/O	FT	PF12	FSMC_A6	-
51	VSS_6	S	–	VSS_6	-	-
52	VDD_6	S	–	VDD_6	-	-
53	PF13	I/O	FT	PF13	FSMC_A7	-
54	PF14	I/O	FT	PF14	FSMC_A8	-
55	PF15	I/O	FT	PF15	FSMC_A9	-
56	PG0	I/O	FT	PG0	FSMC_A10	-
57	PG1	I/O	FT	PG1	FSMC_A11	-
58	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
59	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
60	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
61	VSS_7	S	–	VSS_7	-	-
62	VDD_7	S	–	VDD_7	-	-
63	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
64	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
65	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
66	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
67	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
68	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
69	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX	TIM2_CH3
70	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX	TIM2_CH4
71	VSS_1	S	–	VSS_1	-	-
72	VDD_1	S	–	VDD_1	-	-
73	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/ I2C2_SMBA/USART3_CK/ TIM1_BKIN	-
74	PB13	I/O	FT	PB13	SPI2_SCK/I2S2_CK/ USART3_CTS/TIM1_CH1N	-
75	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS/TIM12_CH1	-

76	PB15	I/O	FT	PB15	SPI2_MOSI/I2S2_SD/ TIM1_CH3N/TIM12_CH2	-
77	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
78	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
79	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
80	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
81	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1/ USART3_RTS
82	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
83	VSS_8	S	_	VSS_8	-	-
84	VDD_8	S	_	VDD_8	-	-
85	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
86	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
87	PG2	I/O	FT	PG2	FSMC_A12	-
88	PG3	I/O	FT	PG3	FSMC_A13	-
89	PG4	I/O	FT	PG4	FSMC_A14	-
90	PG5	I/O	FT	PG5	FSMC_A15	-
91	PG6	I/O	FT	PG6	FSMC_INT2	-
92	PG7	I/O	FT	PG7	FSMC_INT3	-
93	PG8	I/O	FT	PG8	-	-
94	VSS_9	S	_	VSS_9	-	-
95	VDD_9	S	_	VDD_9	-	-
96	PC6	I/O	FT	PC6	I2S2_MCK/TIM8_CH1/ SDIO_D6	TIM3_CH1
97	PC7	I/O	FT	PC7	I2S3_MCK/TIM8_CH2/ SDIO_D7	TIM3_CH2
98	PC8	I/O	FT	PC8	TIM8_CH3/SDIO_D0	TIM3_CH3
99	PC9	I/O	FT	PC9	TIM8_CH4/SDIO_D1	TIM3_CH4
100	PA8	I/O	FT	PA8	USART1_CK/TIM1_CH1/ MCO	-
101	PA9	I/O	FT	PA9	USART1_TX/TIM1_CH2	-
102	PA10	I/O	FT	PA10	USART1_RX/TIM1_CH3	-
103	PA11	I/O	-	PA11	USART1_CTS/USBDM CAN_RX/TIM1_CH4	-
104	PA12	I/O	-	PA12	USART1_RTS/USBDP/ CAN_TX/TIM1_ETR	-
105	PA13	I/O	FT	JTMS-SWDIO	-	PA13
106	Not Connected					-

107	VSS_2	S	_	VSS_2	-	-
108	VDD_2	S	_	VDD_2	-	-
109	PA14	I/O	FT	JTCK-SWCLK	-	PA14
110	PA15	I/O	FT	JTDI	SPI3_NSS/I2S3_WS	TIM2_CH1_ETR/PA15/SPI1_NSS
111	PC10	I/O	FT	PC10	UART4_TX/SDIO_D2	USART3_TX
112	PC11	I/O	FT	PC11	UART4_RX/SDIO_D3	USART3_RX
113	PC12	I/O	FT	PC12	UART5_TX/SDIO_CK	USART3_CK
114	PD0	I/O	FT	PD0	FSMC_D2	CAN_RX
115	PD1	I/O	FT	PD1	FSMC_D3	CAN_TX
116	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX SDIO_CMD	-
117	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
118	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
119	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
120	VSS_10	S	_	VSS_10	-	-
121	VDD_10	S	_	VDD_10	-	-
122	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX
123	PD7	I/O	FT	PD7	FSMC_NE1/FSMC_NCE2	USART2_CK
124	PG9	I/O	FT	PG9	FSMC_NE2/FSMC_NCE3	-
125	PG10	I/O	FT	PG10	FSMC_NCE4_1/FSMC_NE3	-
126	PG11	I/O	FT	PG11	FSMC_NCE4_2	-
127	PG12	I/O	FT	PG12	FSMC_NE4	-
128	PG13	I/O	FT	PG13	FSMC_A24	-
129	PG14	I/O	FT	PG14	FSMC_A25	-
130	VSS_11	S	_	VSS_11	-	-
131	VDD_11	S	_	VDD_11	-	-
132	PG15	I/O	FT	PG15	-	-
133	PB3	I/O	FT	JTDO	SPI3_SCK/I2S3_CK	PB3/TRACESWO TIM2_CH2/SPI1_SCK
134	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4/TIM3_CH1/ SPI1_MISO
135	PB5	I/O	_	PB5	I2C1_SMBA/SPI3_MOSI /I2S3_SD	TIM3_CH2/ SPI1_MOSI
136	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
137	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2	USART1_RX

					/ FSMC_NADV	
138	BOOT0	I	_	BOOT0	-	_
139	PB8	I/O	FT	PB8	TIM4_CH3/SDIO_D4/ TIM10_CH1	I2C1_SCL/CAN_RX
140	PB9	I/O	FT	PB9	TIM4_CH4/SDIO_D5/ TIM11_CH1	I2C1_SDA/CAN_TX
141	PE0	I/O	FT	PE0	TIM4_ETR/FSMC_NB L0	-
142	PE1	I/O	FT	PE1	FSMC_NBL1	-
143	VSS_3	S	_	VSS_3	-	-
144	VDD_3	S	_	VDD_3	-	-

4 Electrical characteristics

Parameter conditions

Unless otherwise specified, all voltages are referenced to VSS.

4.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency by tests in production on 100% of the devices with an ambient temperature at TA = 25℃.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

4.1.2 Typical values

Unless otherwise specified, typical data are based on TA=25℃, VDD=3.3V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

4.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 3.

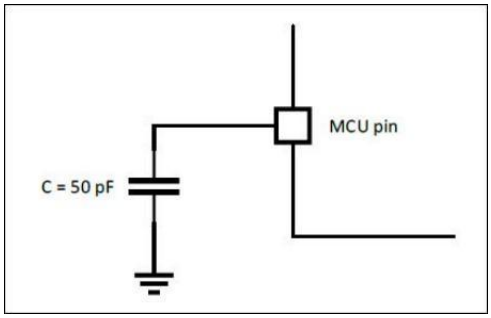


Figure 5 Pin loading conditions

4.1.5 Pin input voltage

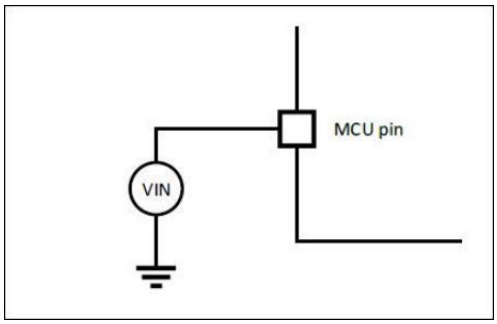


Figure 6 Pin input voltage

4.1.6 Power supply scheme

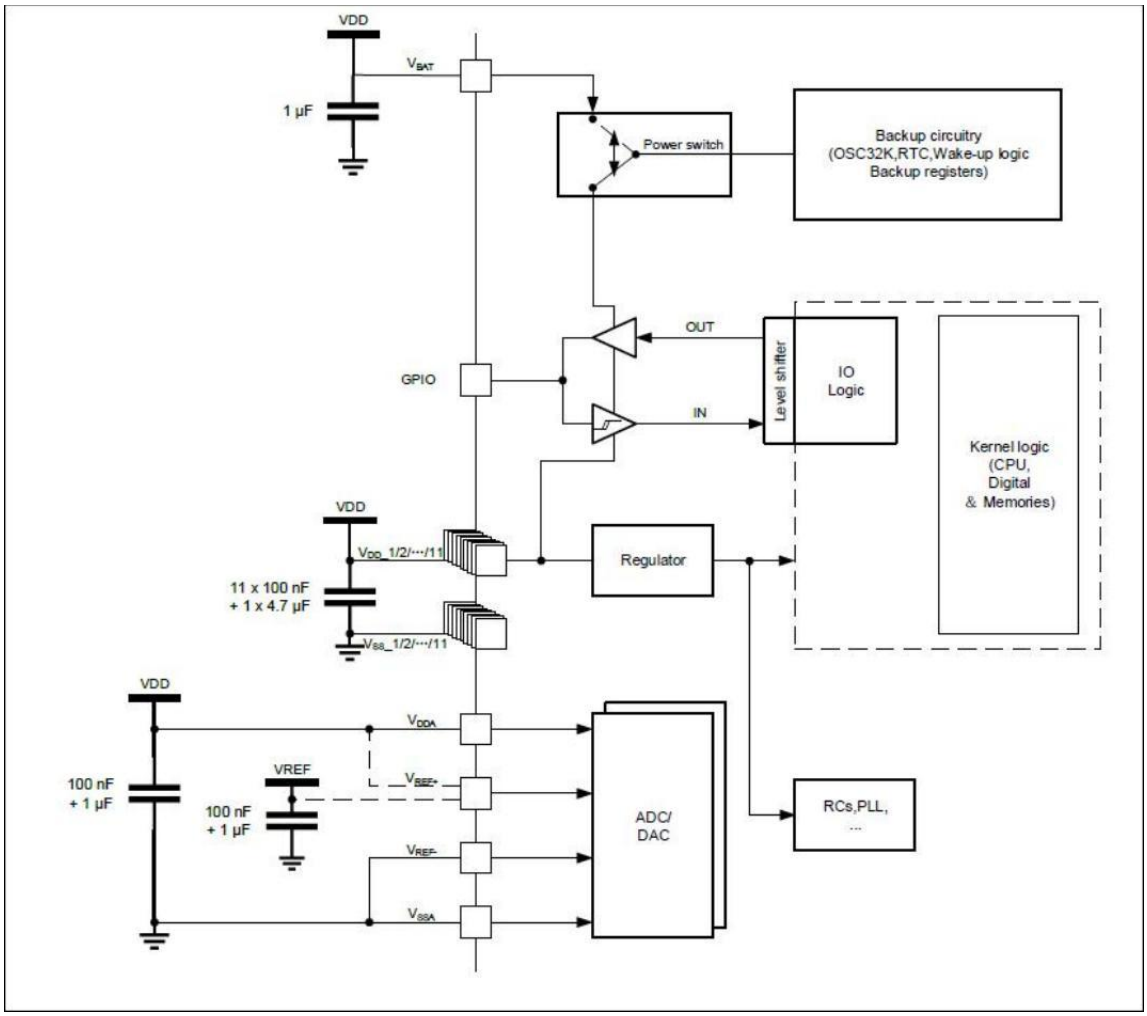


Figure 7 Power supply scheme

4.1.7 Current consumption measurement

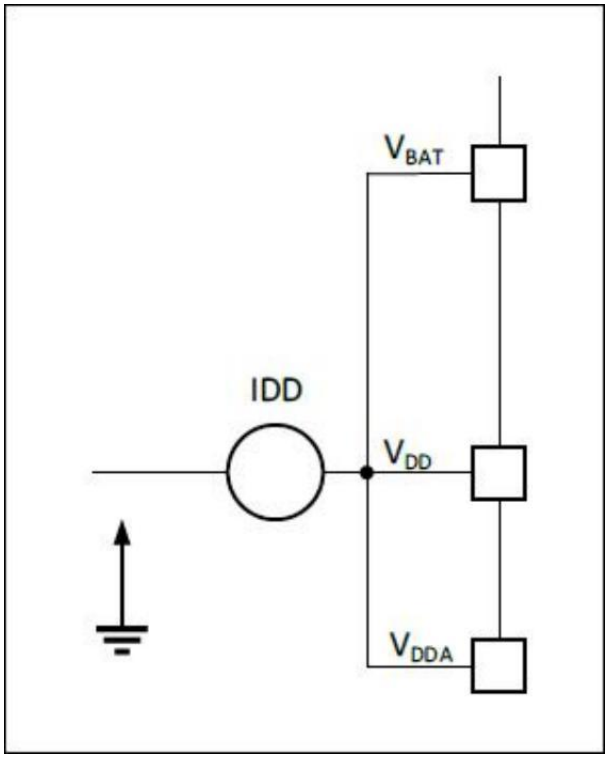


Figure 8 Current consumption measurement

Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 8, 9, 10 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8 Voltage characteristics

Symbol	Description	Min	Max	Unit
VDD - VSS	External main supply voltage(including VDDA and VDD)(1)	-0.3	4	V
VIN	Input voltage on 5V tolerant pin(2)	Vss-0.3	Vdd+4.0	
	Input voltage on any other pin(2)	Vss-0.3	4.0	
|ΔVDDx|	Variations between different VDD power pins	—	50	mV
|VSSx-VSS|	Variations between all the different ground pins	—	50	

(1) All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.

(2) Contains the VREF-feet.

Table 9 Current characteristics

Symbol	Description	Max (1)	Unit
IVDD	Total current into VDD/VDDA power lines (source) (1)	150	mA
IVSS	Total current out of VSS ground lines (sink) (1)	150	
IIO	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	

(1) All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.

Table 10 Temperature characteristics

Symbol	Description	Value	Unit
TSTG	Storage temperature range	-65 ~ +150	℃
TJ	Maximum junction temperature	105	℃

Operating conditions

4.1.8 General operating conditions

Table 11 General operating conditions

Symbol	Parameter	Condition	Min	Max	Unit
fHCLK	Internal AHB clock frequency	—	0	216	MHz
fPCLK1	Internal APB1 clock frequency	—	0	108	
fPCLK2	Internal APB2 clock frequency	—	0	216	
VDD	Standard operating voltage	—	2.0	3.6	V
VDDA(1)	Analog part operating voltage	Must be same with VDD (1)	2.0	3.6	V
VBAT	Backup part operating voltage		1.6	3.6	V
TA	Ambient temperature	—	-40	85	℃

(1) It is recommended to power VDD and VDDA from the same source.

4.1.9 Operating conditions at power-up / power-down

The parameters given in the table below are derived from the ambient temperature listed in Table 10.

Table 12 Operating conditions at power-up / power-down

Symbol	Parameter	Condition	Min	Max	Unit
tVDD	VDD rise time rate	—	0	∞	us/V
	VDD fall time rate		20	∞	

4.1.10 Embedded reset and power control block characteristics

The parameters given in the table below are derived from the ambient temperature listed in Table 8 and the VDD power supply voltage listed in Table 8.

Table 13 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit

VPVD	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.16	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.07	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.26	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.17	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.35	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.26	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.36	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.55	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.45	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.66	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.57	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.76	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.67	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.85	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.77	2.9	V
VPVDhyst(1)	PVD hysteresis	—	—	100	—	mV
VPOR/PDR	Power on/power down reset threshold	falling edge	—	1.90	—	V
		rising edge	—	2.02	—	V
VPDRhyst(1)	PDR hysteresis	—	—	30	—	mV
TRSTTEMPO(1)	Reset temporization	—	—	2	—	ms

(1)Guaranteed by design.

4.1.11 Embedded reference voltage

The parameters given in the table below are derived from the ambient temperature listed in Table 10 and the VDD power supply voltage listed in Table 8.

Table 14 Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VREFINT	Internal reference voltage	-40℃ < TA < +85℃	1.16	1.20	1.24	V
TS_vrefint(1)	ADC sampling time when reading the internal reference voltage	—	—	5.1	17.1	us
TCoeff (2)	Temperature coefficient	—	—	—	100	ppm/℃

(1)Shortest sampling time can be determined in the application by multiple iterations.

(2)Guaranteed by design.

4.1.12 Supply current characteristics

The current consumption is a composite indicator of several parameters and factors such as the operating voltage, ambient temperature, I/Opin loading, device software configuration, operating frequencies, I/Opin switching rate, program location in memory and executed binary code, etc.

The current consumption is measured as described in the Test Conditions chapter.

Current consumption

The MCU is placed under the following conditions:

- All I/Opins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned
- When the peripherals are enabled: fPCLK1 = fHCLK/2 , fPCLK2 = fHCLK

Table 15 Current consumption in Run mode

Symbol	Parameter	Conditions	fHCLK	Typ(1)		Max(2)		Unit
				All peripherals enabled	All peripherals disabled	All peripherals enabled	All peripherals disabled	
IDD	Supply current in Run mode	External clock(3)	216MHz	36.29	25.49	38.50	27.56	mA
			168MHz	27.71	19.27	29.95	21.35	
			72MHz	13.09	9.38	14.93	11.21	
			48MHz	9.35	6.93	11.18	8.74	
			32MHz	6.88	5.25	8.68	7.04	
			24MHz	5.67	4.46	7.41	6.20	
			16MHz	4.43	3.63	6.16	5.34	
			8MHz	3.28	2.58	4.98	4.54	

		Runs on high-speed internal RC oscillator (HSI)	128MHz	21.64	15.19	23.89	17.27	mA
			72MHz	13.03	9.39	15.03	11.31	
			48MHz	9.34	6.92	11.26	8.78	
			32MHz	7.55	5.73	8.73	7.08	
			24MHz	5.69	4.49	7.74	6.24	
			16MHz	4.45	3.66	6.21	5.39	
			8MHz	3.30	3.88	5.02	4.57	

(1)The typical value is obtained by testing at TA=25℃, VDD=3.3V.

(2)The maximum value is obtained by testing at TA=85℃, VDD=3.6V.

(3)The external clock is 8MHz, and the PLL is enabled when fHCLK>8MHz.

Table 16 Current consumption in Sleep mode, code running from flash

Symbol	Parameter	Conditions	fHCLK	Typ(1)		Max(2)		Unit
				All peripherals enabled	All peripherals disabled	All peripherals enabled	All peripherals disabled	
IDD	Supply current in Sleep mode	External clock(3)	216MHz	25.72	7.01	27.73	8.70	mA
			168MHz	19.46	4.81	21.49	6.58	
			72MHz	9.53	3.25	11.31	4.92	
			48MHz	6.99	2.81	8.76	4.51	
			32MHz	5.32	2.54	7.07	4.23	
			24MHz	4.50	2.41	6.22	4.09	
			16MHz	3.66	2.28	5.36	3.96	
			8MHz	2.90	2.17	4.57	3.84	
		Runs on high-speed internal RC oscillator (HSI)	128MHz	15.31	4.14	17.36	5.90	mA
			72MHz	9.47	3.20	11.36	4.93	
			48MHz	6.97	2.80	8.80	4.52	
			32MHz	5.32	2.54	7.11	4.26	
			24MHz	4.49	2.41	6.25	4.12	
			16MHz	3.65	2.27	5.39	3.98	
			8MHz	2.89	2.17	4.61	3.87	

(1)The typical value is obtained by testing at TA=25℃, VDD=3.3V.

(2)The maximum value is obtained by testing at TA=85℃, VDD=3.6V.

(3)The external clock is 8MHz, and the PLL is enabled when fHCLK>8MHz.

Table 17 Typical and maximum current consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)	Max(2)	Unit
IDD	Supply current in Stop mode	Regulator in Run mode, low-speed and high-speed internal RC oscillators and external high-speed oscillator OFF (no independent watchdog)	210	1290	uA
		Regulator in Low-power mode, low-speed and high-speed internal RC oscillators and external high-speed oscillator OFF (no independent watchdog)	150	1220	
	Supply current in Standby mode	Low-speed internal RC oscillator, external low-speed oscillator and RTC, IWDG OFF	0.7	2.2	
		Low-speed internal RC oscillator ON, external low-speed oscillator and RTC, IWDG OFF	1.0	2.5	
		External low-speed oscillator ON, low-speed internal RC oscillator and RTC, IWDG OFF	1.0	2.6	
		External low-speed oscillator and RTC ON, low-speed internal RC oscillator and IWDG OFF	1.3	2.7	
		Low-speed internal RC oscillator and IWDG ON, external low-speed oscillator and RTC OFF	1.0	2.7	
IDD_VBAT	Supply current in backup area	External low-speed oscillator and RTC ON	0.9	1.3	

(1)The typical value is obtained by testing at TA=25℃, VDD=VBAT=3.3V.
(2)The maximum value is obtained by testing at TA=85℃, VDD=VBAT=3.6V.
(3)Derived from comprehensive evaluation, not tested in production.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All I/Opins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned

● The given value is calculated by measuring the current consumption

- ◆ with all peripherals clocked off
- ◆ with only one peripheral clocked on

Table 18 On-chip peripheral current consumption

Peripherals		Typ consumption at 25℃	Unit
APB1	TIM2	2.08	uA/MHz
	TIM3	2.36	
	TIM4	2.22	
	TIM5(2)	2.08	
	TIM6	0.14	
	TIM7	0.14	
	SPI2/I2S(2)	0.97	
	SPI3/I2S(2)	0.83	
	USART2	0.56	
	USART3	0.56	
	UART4(2)	0.56	
	UART5(2)	0.56	
	I2C1	1.81	
	I2C2	1.81	
	USB	5.42	
	CAN	1.11	
	SDIO(2)	7.92	
	WWDG	0.24	
	DAC	0.58	
	PWR	0.008	
	BKP	0.11	
APB2	ADC1(1)	5	
	ADC2(1)	5	
	ADC3(1)(2)	5	
	TIM1	3.71	
	TIM8(2)	3.76	
	SPI1	1.83	
	USART1	1.39	

(1)Specific conditions for measuring ADC current consumption: fHCLK=56MHz, fAPB1=fHCLK/2, fAPB2=

fHCLK, fADCCLK=fAPB2/4, ADON bit in ADC_CR2 register=1。

4.1.13 External clock source characteristics

High-speed external user clock generated from an external oscillator source

The characteristics given in Table 19 result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in Table 8 and Table 10.

Table 19 High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fHSE_ext	User external clock source frequency(1)	—	0.615	8	35	MHz
VHSEH	OSC_IN input pin high level voltage		0.48Vdd	—	Vdd	V
VHSEL	OSC_IN input pin low level voltage		Vss	—	0.38Vdd	
tw(HSE)	OSC_IN high or low time(1)		5	62.5	—	ns
tr(HSE) tf(HSE)	OSC_IN rise or fall time(1)		—	4.1	20	
Cin(HSE)	OSC_IN input capacitance(1)	—	—	5	—	pF
DuCy(HSE)	Duty cycle	—	45	50	55	%

(1)Guaranteed by design.

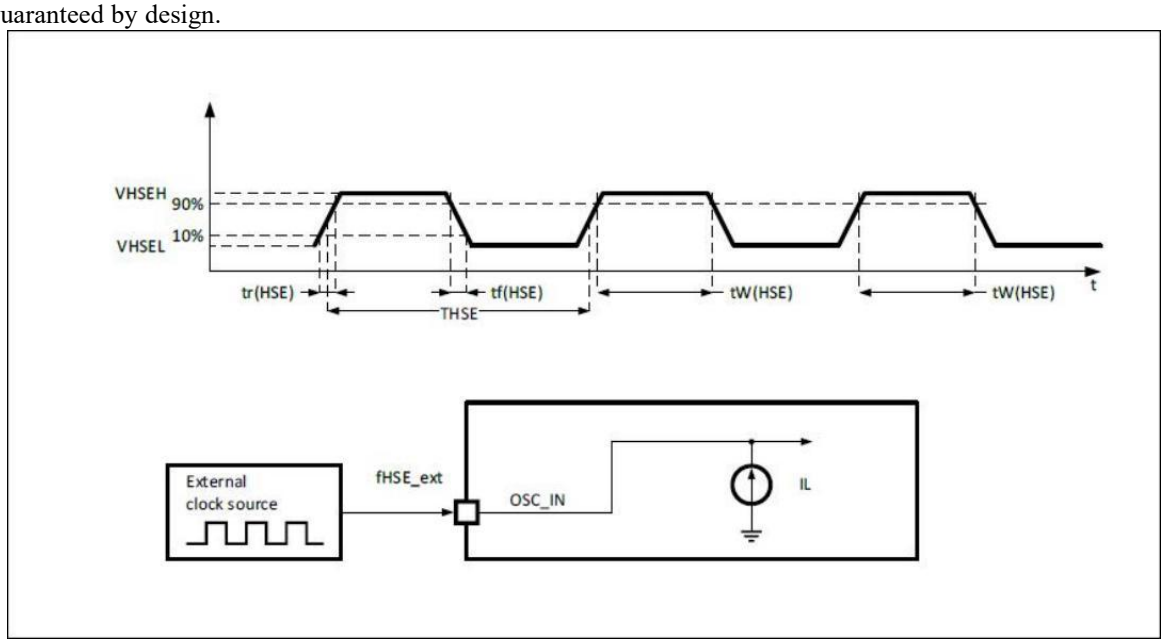


Figure 9 High-speed external clock source AC timing diagram

Low-speed external user clock generated from external oscillator source

The characteristics given in Table 20 result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in Table 8 and Table 10.

Table 20 Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fHSE_ext	User external clock source frequency(1)	—	—	32.768	1000	KHz
VLSEH	OSC32_IN input pin high level voltage		0.48Vdd	—	VDD	V
VLSEL	OSC32_IN input pin low level voltage		VSS	—	0.38Vdd	
tw(LSE) tw(LSE)	OSC32_IN high or low time(1)		450	—	—	ns
tr(LSE) tf(LSE)	OSC32_IN rise or fall time(1)		—	—	50	
Cin(LSE)	OSC32_IN input capacitance(1)	—	—	5	—	pF
DuCy(LSE)	Duty cycle	—	30	—	70	%

(1)Guaranteed by design.

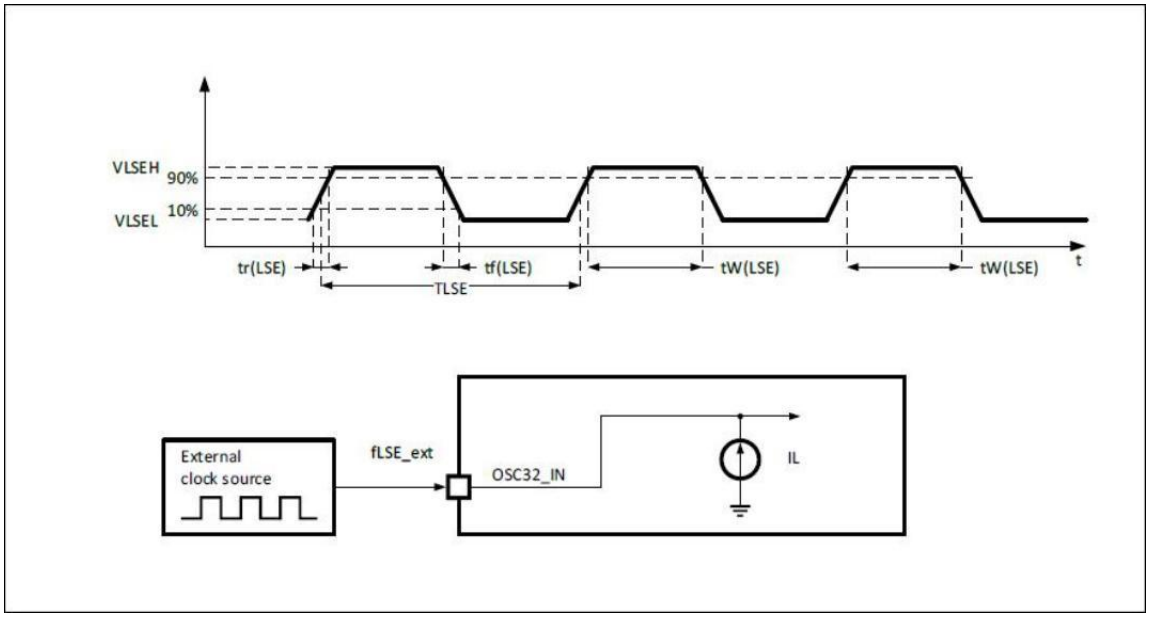


Figure 10 Low-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 19. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics(frequency,

package, accuracy).

Note: The crystal resonator mentioned here is what we usually call passive crystal oscillator.

Table 21 HSE 4~32MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
fOSC_IN	Oscillator frequency	—		4	8	32	MHz
tSU(HSE)(3)	Startup time	VDD is stabilized	TA = -40℃	—	790	—	us
			TA = 25 ℃	—	860	—	
			TA = 85 ℃	—	960	—	

(1) Resonator characteristics given by the crystal/ceramic resonator manufacturer.

(2) Guaranteed based on test during characterization.

(3) tSU(HSE) is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For CL1 and CL2, it is recommended to use high-quality external ceramic capacitors in the 5pF to 25pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. CL1 and CL2 are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2. PCB and MCU pin capacitance must be included (10pF can be used as a rough estimate of the combined pin and board capacitance) when sizing CL1 and CL2.

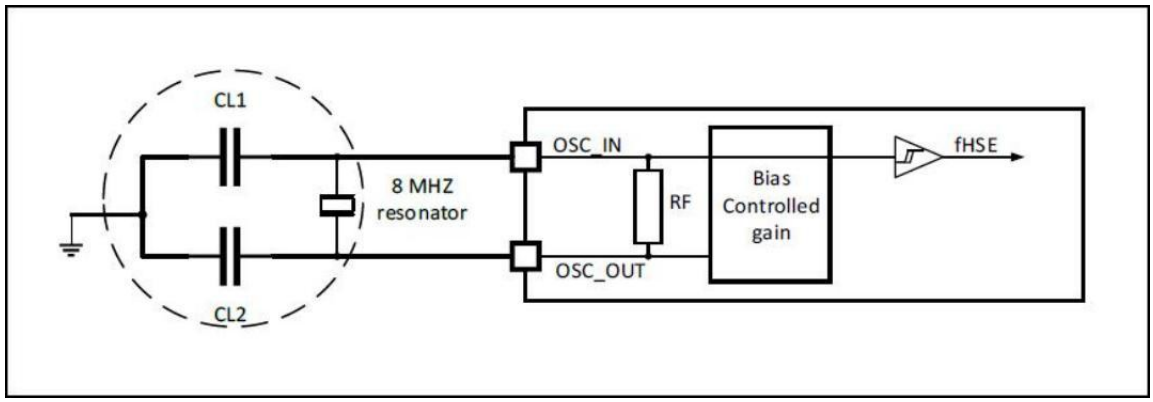


Figure 11 Typical application with an 8 MHz crystal

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Note: The crystal resonator mentioned here is what we usually call passive crystal oscillator.

Table 22 LSE oscillator characteristics (fLSE=32.768kHz)(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
tSU(HSE)(1)	Startup time	VDD is stabilized	TA = -40℃	—	321	—	ms
			TA = 25 ℃	—	221	—	
			TA = 85 ℃	—	223	—	

(1)Guaranteed based on test during characterization.

For CL1 and CL2 it is recommended to use high-quality ceramic capacitors in the 5pF to 15pF range selected to match the requirements of the crystal or resonator. CL1 and CL2, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of CL1 and CL2.

Load capacitance CL has the following formula: CL = CL1 x CL2 / (CL1 + CL2) + Cstray, where Cstray is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2pF and 7pF.

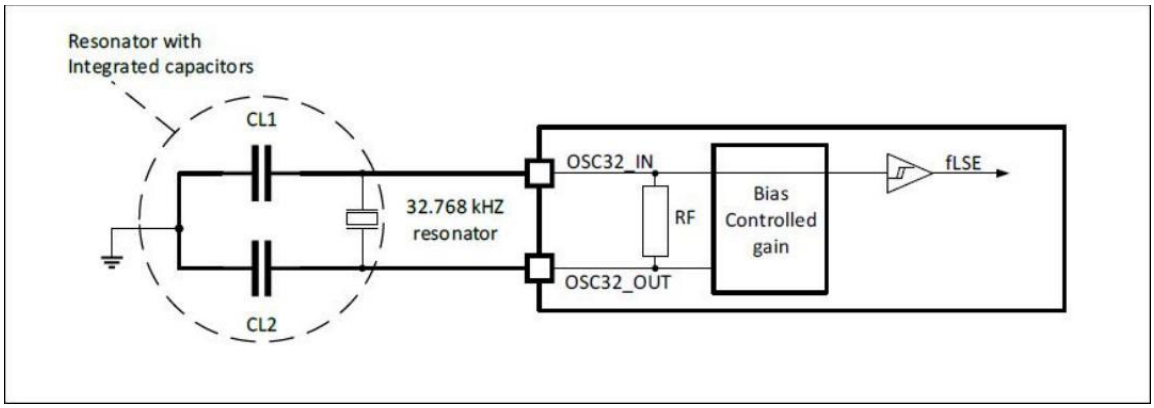


Figure 12 Typical application with a 32.768 kHz crystal

4.1.14 Internal clock source characteristics

The characteristics given in Table 23 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 8 and Table 10.

High-speed internal (HSI) RC oscillator

Table 23 HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fHSI	frequency	—	—	8	—	MHz
ACCHSI	Accuracy of the HSI oscillator	TA = -40~85℃	-2.5	—	2.5	%
tSU(HSI)	HSI oscillator startup time	—	—	12	—	us
IDD(HSI)	HSI oscillator power consumption	—	—	3.5	—	uA

(1)VDD = 3.3V, TA = -40~85℃, unless otherwise specified.

Low-speed internal (LSI) RC oscillator

Table 24 LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fLSI(2)	frequency	—	38	40	42	kHz
tSU(LSI)(3)	LSI oscillator startup time	—	—	75	—	us
IDD(LSI)(3)	HSI oscillator power consumption	—	—	0.28	—	uA

(1)VDD = 3.3V, TA = -40~85℃, unless otherwise specified.

(2)Guaranteed based on test during characterization.

(3)Guaranteed by design.

4.1.15 Wakeup time from low-power mode

The wakeup times is measured on a wakeup phase with a 8MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering sleep mode

All timings are derived from tests performed under ambient temperature

Table 25 Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
tWUSLEEP(1)	Wakeup from sleep mode	10	CPU clock cycle
tWUSTOP(1)	Wakeup from stop mode(regulator in low-power mode)	12	us
tWUSTDBY(1)	Wakeup from standby mode	1600~~(2)/260(3)~~	us

(1)The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

4.1.16 PLL characteristics

The characteristics given in Table 26 are derived from tests performed under ambient temperature and supply voltage conditions summarized

Table 26 PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
fPLL_IN	PLL input clock(2)	1	8	32	MHz
	PLL input clock duty cycle	40	—	60	%

fPLL_OUT	PLL multiplier output clock	4	—	216	MHz
tLOCK	PLL lock time	—	51.2	87.8	us
Jitter	Cycle-to-cycle jitter	—	—	200	ps

(1)Guaranteed based on test during characterization.

(2)Be careful to use the correct multiplier coefficient, so that the fPLL_OUT is within the allowable range according to the PLL input clock frequency.

4.1.17 Memory characteristics

Flash memory

The characteristics are given at TA = –40 to 105 °C unless otherwise specified.

Table 27 Flash memory characteristics

Symbol	Parameter	Conditions	Typ	Unit
tPROG	16-bit programming time	—	50us	us
tERASE	Page erase time	—	25	ms
tME	Mass erase time	—	3/6 (1)	s

Table 28 Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
NEND	Endurance	TA = -40~85℃	100	—	—	kcycles
tRET	Data retention	TA = 105℃	20	—	—	years

(1)Guaranteed based on test during characterization.

4.1.18 Absolute maximum ratings (electrical sensitivity)

Electrostatic discharge(ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test is compliance with the JESD22-A114/C101 standard.

Table 29 ESD absolute maximum ratings

Symbol	Parameter	Conditions	Type	Max(1)	Unit
VESD(HBM)	Electrostatic discharge voltage (human body model)	TA=+25 °C，confirming to JEDEC EIA/JESD22-A114	3A	4000	V

(1)Guaranteed based on test during characterization.

4.1. 19 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 30 are derived from tests performed under the conditions summarized in Table 8 and Table 10. All I/Os are compliance with CMOS and TTL.

Table 30 I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL	Low level input voltage	—		—	1.38	V
VIH	Standard IO input high level voltage		1.59	—	—	
	IO FT(1) input high level voltage		1.59	—	—	
Vhys	Standard IO Schmitt trigger voltage hysteresis(2)	—	—	0.21	—	V
	5V tolerance IO Schmitt trigger voltage hysteresis(2)		—	0.21	—	V
Ilkg	Input leakage current(4)	VSS ≤ VIN ≤ VDD Standard I/Os	—	—	±0.5	uA
		VIN = 5V, 5V tolerance port	—	—	±1	
RPU	Weak pull-up equivalent resistor(5)	VIN = VSS	37	—	38.5	kΩ
RPD	Weak pull-down equivalent resistor(5)	VIN = VDD	43.7	—	45.7	kΩ
CIO	I/O pin capacitance			5		pF

Output voltage

Unless otherwise specified, the parameters given in Table 31 are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in Table 8 and Table 10. All I/Os are CMOS and TTL compliant.

Table 31 Output Voltage Characteristics

Symbol	Parameter	Conditions	Min	Max	Max
VOL	Output low level voltage	TTL port， I_{IO} = +12mA		0.4	V
VOH	Output high level voltage	VDD=3.3V	2.9		
VOL	Output low level voltage	CMOS port， I_{IO} = +14mA		0.4	
VOH	Output high level voltage	VDD=3.3V	2.9		
VOL	Output low level voltage	I_{IO} = +34mA		1.3	
VOH	Output high level voltage	VDD=3.3V	2		

4.1.20 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor

Unless otherwise specified, the parameters given in Table 32 are derived from tests performed under the ambient temperature and VDD supply voltage conditions summarized in Table 8 and Table 10.

Table 32 NRST pin characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
VIL(NRST)(1)	NRST Input low level voltage	—	—	1.31	—	V
VIH(NRST)(1)	NRST Input high level voltage	—	—	1.57	—	
Vhys(NRST)	NRST Schmitt trigger voltage hysteresis	—	—	260	—	mV
RPU	Weak pull-up equivalent resistor(2)	VIN=VSS	—	37	—	kΩ
VF(NRST)(1)	NRST Input filtered pulse	—	—	120	—	ns
VNF(NRST)(1)	NRST Input not filtered pulse	—	25	—	—	ns

(1)Guaranteed by design.

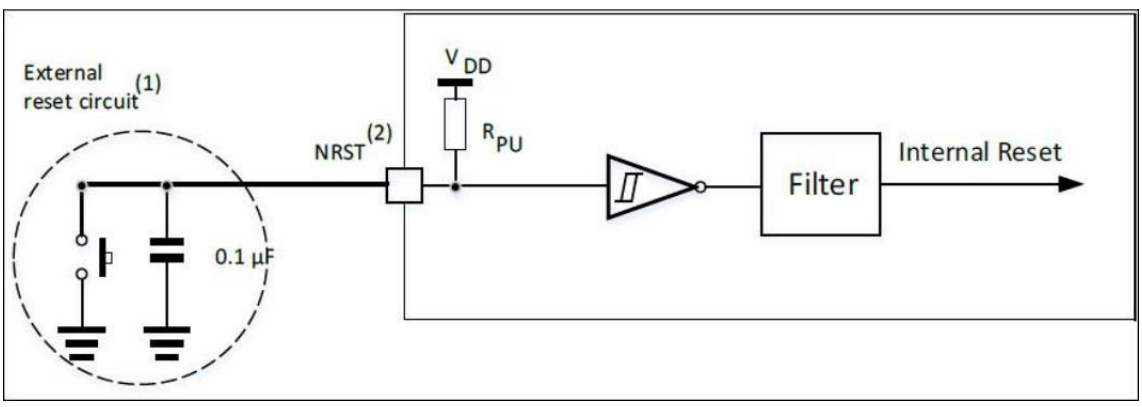


Figure 13 Recommended NRST pin protection

(1)The reset network protects the device against parasitic resets.

(2)The user must ensure that the level on the NRST pin can go below the VIL(NRST) max level specified in Table 32. Otherwise the MCU cannot be reset

4.1.21 TIM timer characteristics

The parameters given in Table 33 are guaranteed by design.

Table 33 TIMx characteristics

Symbol	Parameter	Min	Max	Unit
tres(TIM)	Timer resolution time	1	—	tTIMxCLK
fEXT	Timer external clock frequency on CH1 to CH4	0	FTIMCLK/2	MHz
ResTIM	Timer resolution	—	16	bit
tCOUNTER	16-bit counter clock period when internal clock is selected	1	65535	tTIMxCLK
tMAX_COUNT	Maximum possible count	—	65535*65535	tTIMxCLK

4.1.22 CAN (controller area network) interface

Refer to Section 4.3.12 I/O port characteristics chapter for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX)

4.1.23 12-bit ADC characteristics

Unless otherwise specified, the parameters given in Table 34 are derived from tests performed under the ambient temperature, fPCLK2 frequency and VDDA supply voltage conditions summarized in Table 8 and Table 10.

Note: It is recommended to perform a calibration after eachpower-up.

Table 34 ADC characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
VDDA	Power supply	—	2.0	3.3	3.6	V
VREF+	Positive reference voltage	—	2.0	—	VDDA	V
fADC	ADC clock frequency	—	0.6	—	14	MHz
fS(2)	Sampling rate	—	0.05	—	1	MHz

fTRIG(2)	External trigger frequency	fADC = 14MHz	—	—	823	kHz
VAIN	Conversion voltage range(3)	—	0		VREF+	V
RAIN(2)	External input impedance	—	—	—	50	kΩ
RADC(2)	Sampling switch resistance	—	—	—	1	kΩ
CADC(2)	Internal sample and hold capacitor	—	—	—		pF
tCAL(2)	Calibration time	fADC = 14MHz	5.9			us
			83			1/fADC
tlat(2)	Injection trigger conversion latency	fADC = 14MHz	—	—	0.214	us
			—	—	3	1/fADC
tlatr(2)	Regular trigger conversion latency	fADC = 14MHz	—	—	0.143	us
			—	—	2	1/fADC
tS(2)	Sampling time	fADC = 14MHz	0.107	—	17.1	us
			1.5	—	239.5	1/fADC
tSTAB(2)	Power-up time	—	0	0	1	us
tCONV(2)	Total conversion time (including sampling time)	fADC = 14MHz			18	us
			14 to 252 (tS for sampling +12.5 for successive approximation)			1/fADC

(1)Guaranteed by the comprehensive assessment.

(2)Guaranteed by design.

(3)According to different package, VREF+ is internally connected to VDDA, VREF- is internally connected to VSSA, see chapter 3 for details.

(4)For external triggers, a delay of 1/fPCLK2 must be added to the latency specified in Table 34.

Table 35 RAIN max for fADC = 14MHz(1)

TS(cycles)	tS(us)	Max RAIN(kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50

71.5	5.11	-
239.5	17.11	-

(1)Guaranteed by design.

4.1.24 DAC electrical parameters

Table 36 DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Remark
VDDA	Analog supply voltage	2.0	-	3.6V	V	
VREF+	Reference voltage	2.0	-	3.6V	V	VREF+ must always be lower than VDDA
VSSA	Ground wire	0	-	0	V	-
RLOAD(1)	Load resistance with buffer open	5	-	-	kΩ	-
RO(2)	Output impedance with buffer off	-	-	15	kΩ	-
CLOAD(1)	Load capacitance	-	-	50	pF	Bulk capacitor on DAC_OUT pin (buffer on)
DAC_OUTsmall(1)	DAC_OUT voltage on low side when buffer is on	50	-	-	mV	Gives the maximum DAC output span
DAC_OUTbig(1)	DAC_OUT voltage on high side when buffer is on	-	-	VREF+ - 0.2	V	
DAC_OUTsmall(1)	DAC_OUT voltage on low side with buffer off	-	0.5	-	mV	Gives the maximum DAC output span
DAC_OUTbig(1)	DAC_OUT voltage on high side with buffer off	-	-	VREF+ - 0.03	V	
DNL(2)	Nonlinear distortion (deviation between 2 consecutive codes - 1LSB)	-	-	+-2	LSB	DAC configured as 12-bit
INL(2)	Nonlinear accumulation (deviation between the value measured at code i and the line between code DAC_OUT large	-	-	+-4	LSB	DAC configured as 12-bit

	and code DAC_OUT small)					
Offset Error(2)	Offset error (the deviation between the measured value at code 0x800 and the ideal value V REF+ /2)	-	15	25	mV	With VREF+ = 3.3 V, the DAC is configured as 12-bit
tSETTLING	Setup time (full scale: 10-bit input code transitions from small to large, DAC_OUT reaches ±1 LSB of its final value)	-	3	4	us	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ
Update rate	When the input code is a small change (from the value i to i+1 LSB), the large frequency of the correct DAC_OUT is obtained	-	-	1	MS/s	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ
tWAKEUP	Time to wake up from off state (set ENx bit in DAC control register)	-	6.5	10	us	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ input code between small and large possible values
PSRR+ (1)	Supply rejection ratio (relative to VDDA) (static DC measurement)	-	-60	-50	dB	Without R LOAD , C LOAD ≤ 50 pF

(1)Guaranteed by design.

(2)Guaranteed by the comprehensive assessment.

4.1.25 Temperature sensor characteristics

Table 37 Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Avg_Slope(1)	Average slope	—	5	—	mV/°C
V25(1)	Voltage at 25 °C	—	1.43	—	V
tSTART(2)	Startup time	—	—	10	us
TS_temp(2)(3)	ADC sampling time when	—	—	17.1	us

	reading the temperature				

(1)Guaranteed by design.

(2)Guaranteed by the comprehensive assessment.

(3)Shortest sampling time can be determined in the application by multiple iterations.

(4)For HL2103ACCT6, HL2103ARPT6

(5)For HL2103ACBT6

Use the following formula to find the temperature:：

Temperature(°C) = {(V25 – VSENSE) / Avg_Slope} +25

Note(1)：

V25 = value of VSENSE at 25 °C

Avg_Slope = Average slope of the temperature vs. VSENSE curve (in mV/°C)

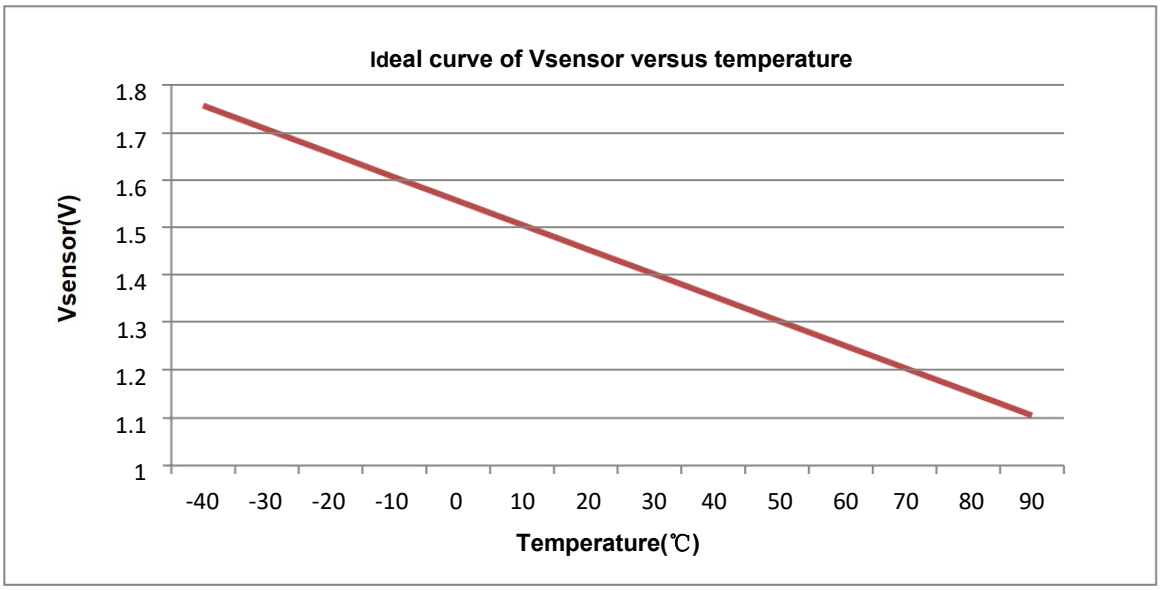
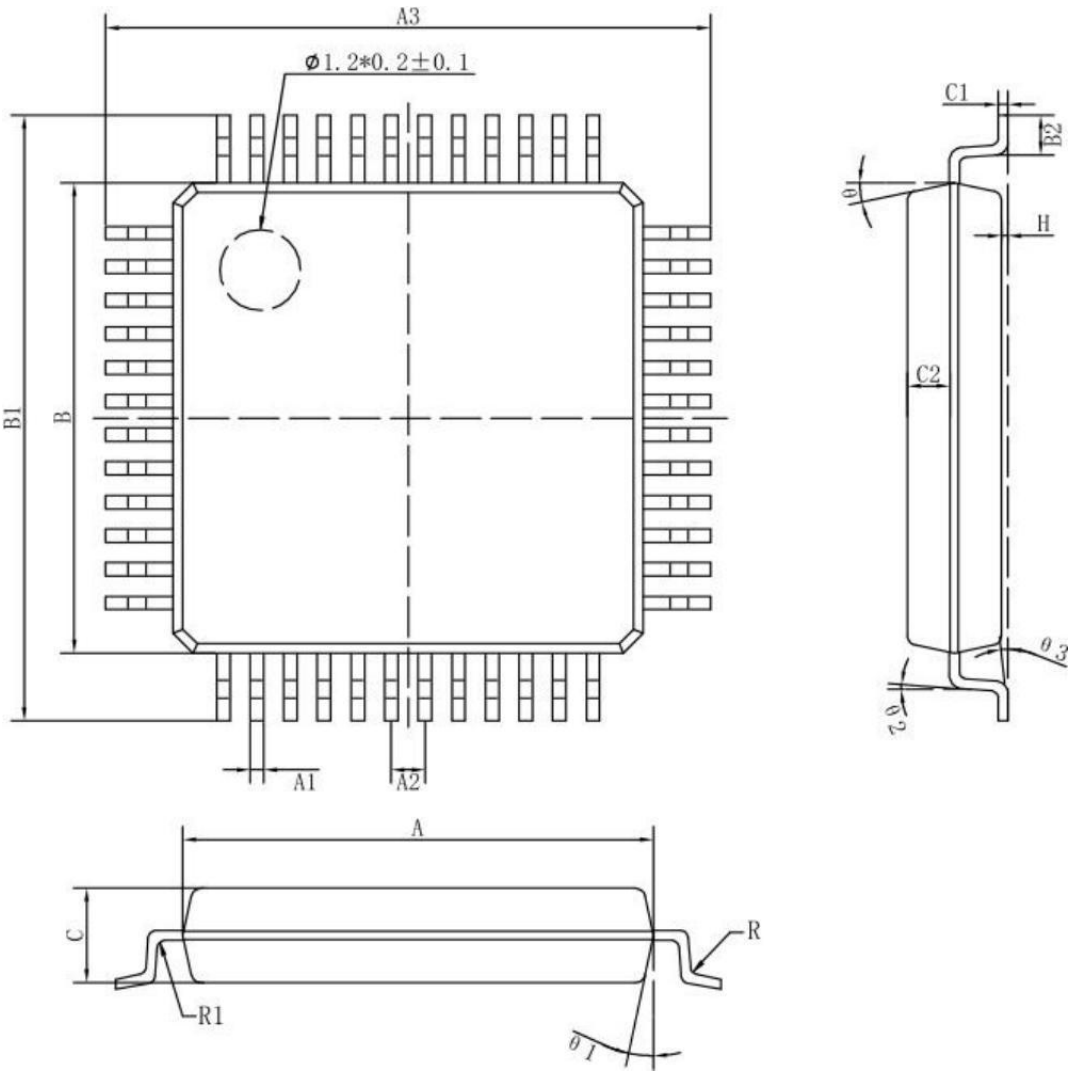


Figure 14 Ideal curve of V SENSE versus temperature(1)

5 Package Information

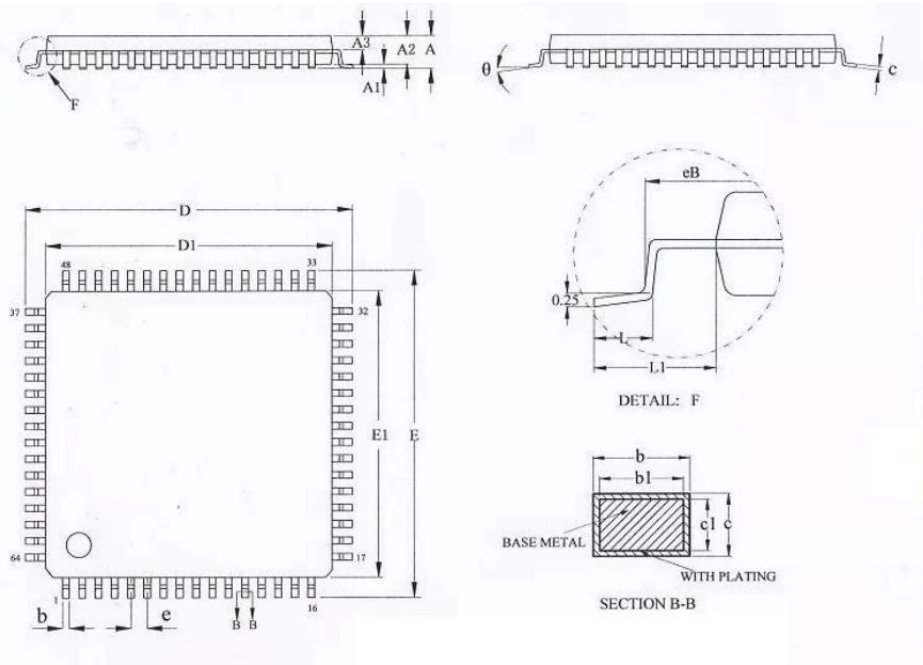
LQFP48 package



尺寸 / 标注	最小(mm)	最大(mm)	尺寸 / 标注	最小(mm)	最大(mm)
A	6.90	7.10	C2	0.636TYP	
A1	0.20TYP		H	0.05	0.15
A2	0.50TYP		θ	12° TYP4	
A3	8.80	9.20	θ1	12° TYP4	
B	6.90	7.10	θ2	4° TYP	
B1	8.80	9.20	θ3	0° ～ 5°	
B2	0.50	0.80	R	0.15TYP	
C	1.30	1.50	R1	0.12TYP	
C1	0.127	0.16			

Figure 15 LQFP48 7mm×7mm package size

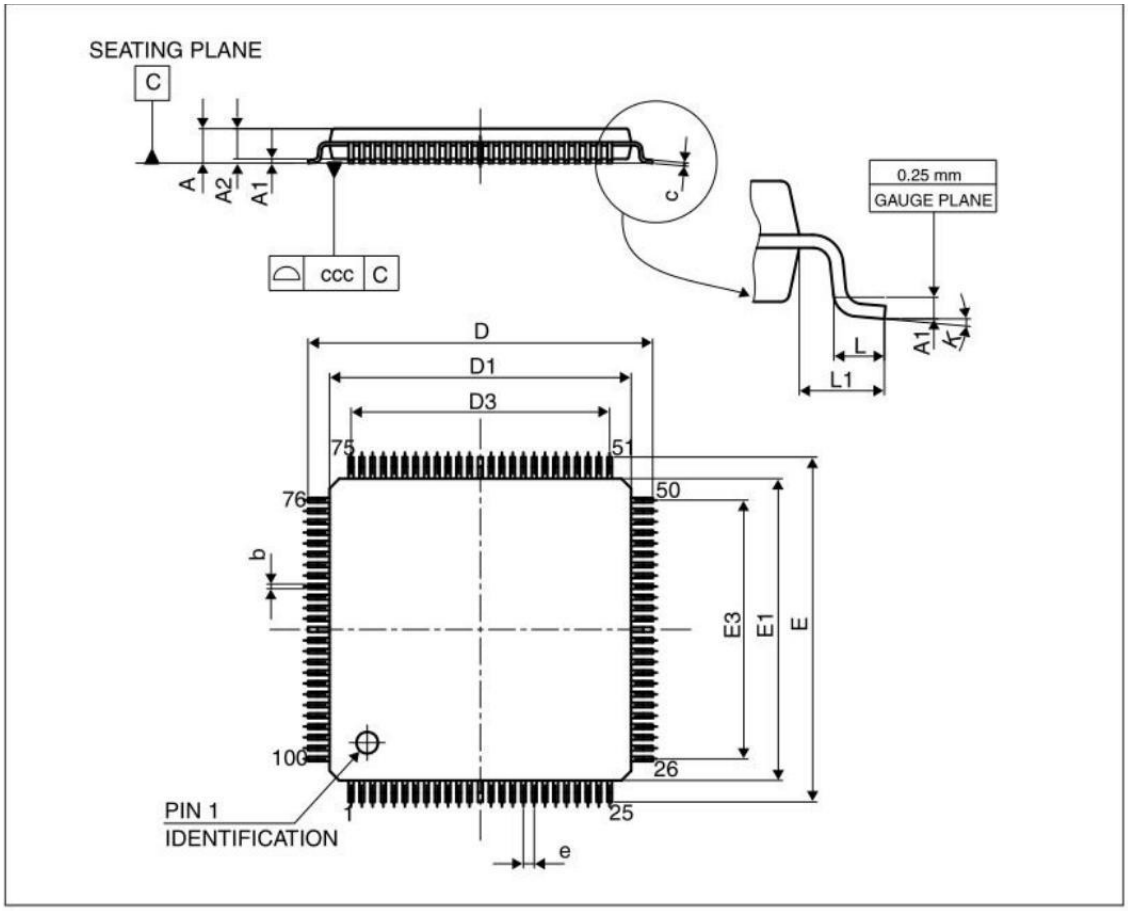
LQFP64 package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
eB	11.05	—	11.25
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Figure 16 LQFP64 10mm×10mm package size

LQFP100 package



Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

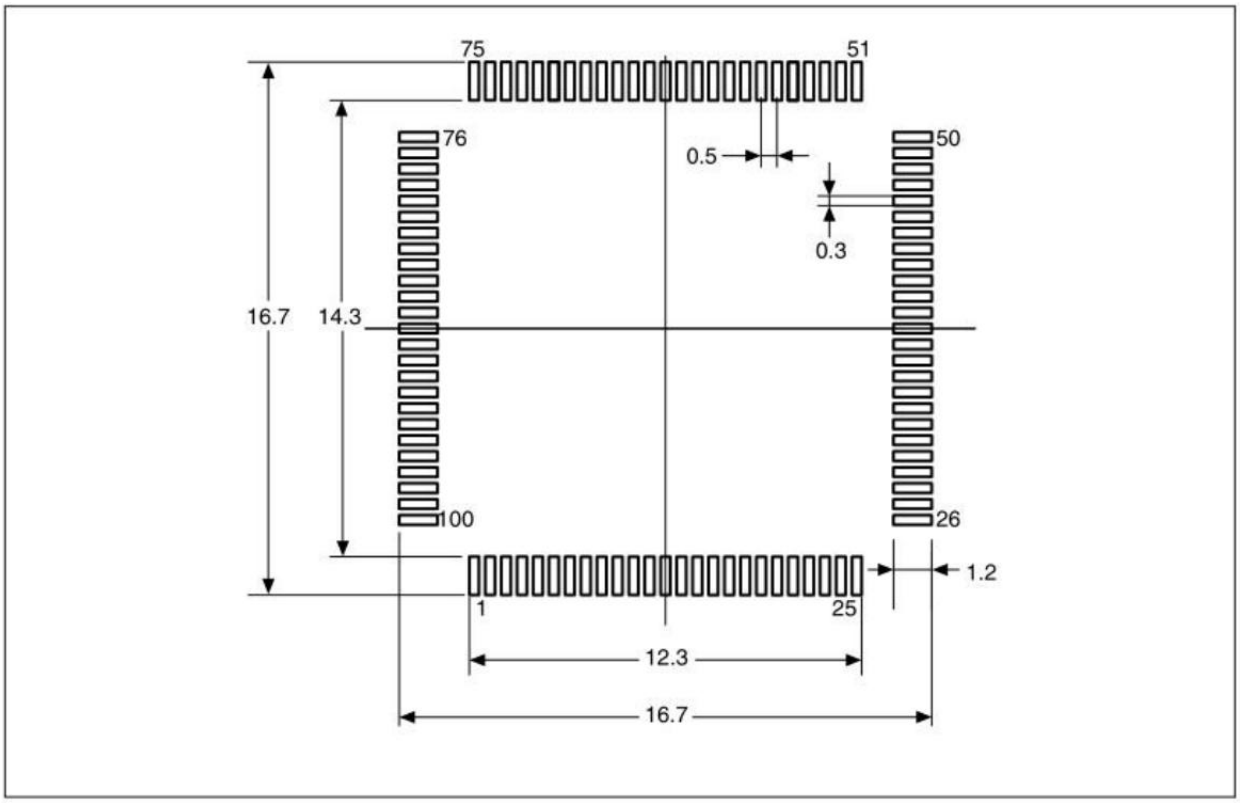
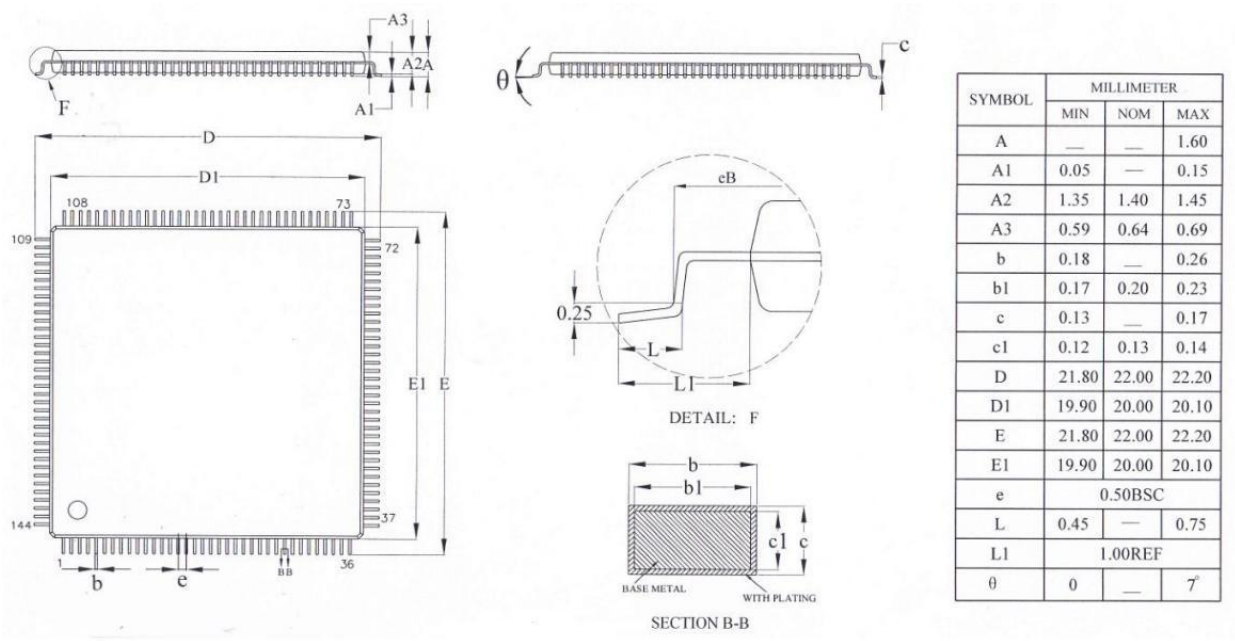


Figure 17 LQFP100 14mm×14mm package size

LQFP144 package



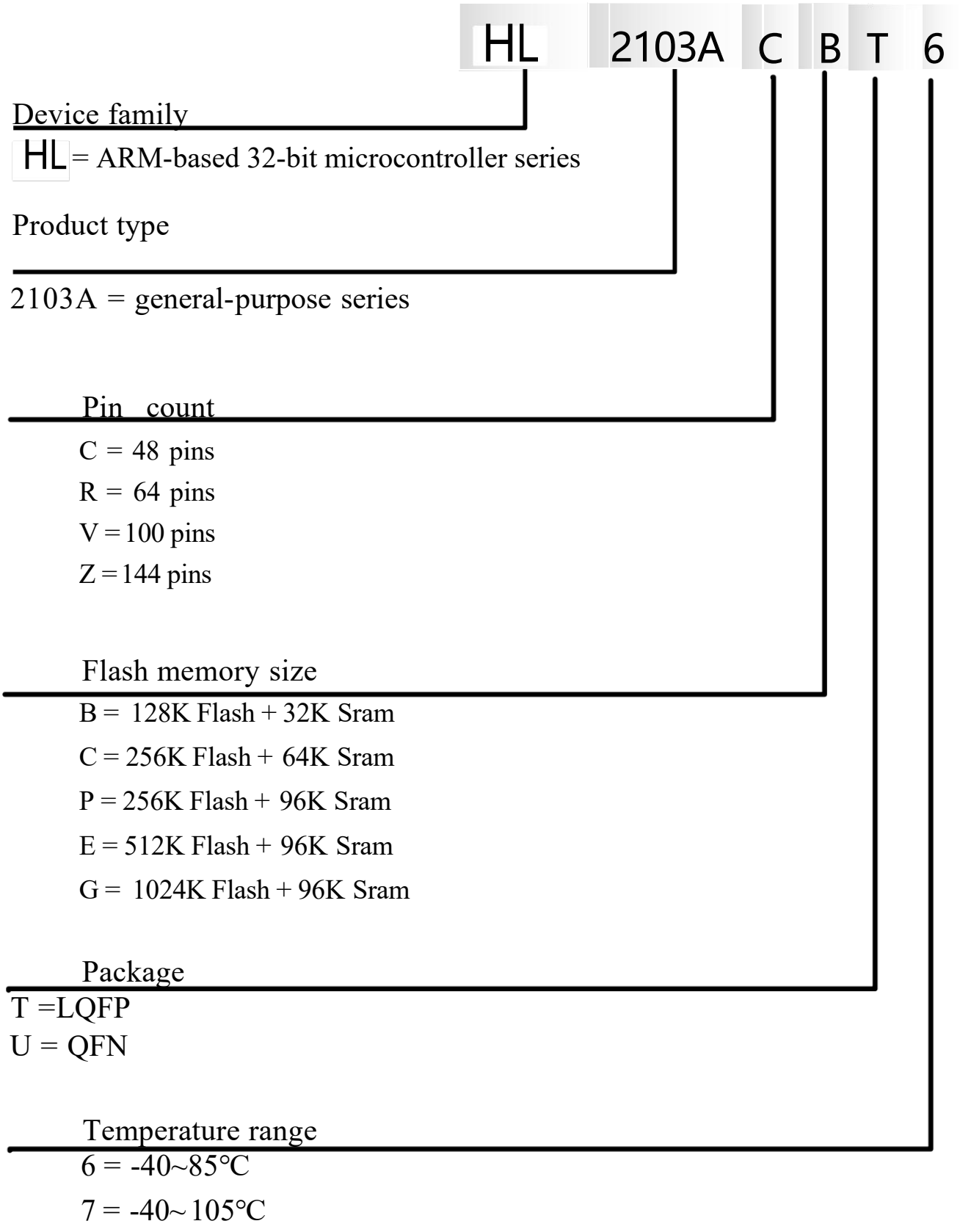
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Figure 18 LQFP144 20mm×20mm package size

6 Ordering information scheme

Table 38 HL2103A Ordering information scheme

Example:



7 Revision history

Table 39 Document revision history

Date	Revision	Changes
2021-1-17	1.00	Initial release
2022-5-28	1.01	Added LQFP100 package description
2022-7-20	1.02	Added LQFP144 package description
2022-7-27	1.03	Added LQFP100 package, HL2103A description
2023-3-09	1.04	Added LQFP144 package, HL2103A description